ELECTRICAL TEST METHOD ADVANCES ON SPECIFIC COMPONENTS AND THEIR RESPONSE TO THE ENVIRONMENT

ABSTRACT

As components reduce in size, the electrical clearance between conductors creates a reliability concern when flux residues are present. Since the area under these components is tiny, chemical extraction is no longer a reliable method for determining cleanliness levels. This problem finds a growing need to understand the impacts of residues left from the flux and other process chemistries on site-specific components. Since these residues can lead to premature failure of assemblies once in the field, an electrical test method on site-specific components and their response to the environment is needed.

Computing power provides transformational importance in catching problems and diagnosing the impact of residues left under leadless and bottom terminated components used on production hardware. An emerging trend is known as the "Digital Twin," provides a dynamic software model of a physical thing or system to conceive, develop, and validate a process. Using physics data on how the components on the electronic circuitry operate and respond to the environment, a digital twin can be used to analyze and simulate real-world conditions, develop data to detect process creep, improve operations and add value.

The purpose of this research is to develop a digital replica of electronic components used on production hardware, maintained as a virtual equivalent throughout the lifespan of the physical product. The test instrument uses sensors and other data to analyze the impact of residues trapped under the components bottom termination. The real-time data analytics allows the engineer to respond to changes at the assembly site and to improve conditions. The value is from moving away from test methods that provide a weak correlation to almost exact design time and run time clone.

Keywords: Bottom Terminated Components, Electrochemical Migration, Dendritic Growth, J-STD-001G, Amendment 1, Flux Residues, Reliability, Warranty, Surface Insulation Resistance

INTRODUCTION

The Resistivity of Solvent Extract (ROSE) test was developed back in the '70s by the defense industry to measure ionic contamination on printed circuit boards. The test method has been used since its inception to measure acceptable and unacceptable cleanliness of the PCB following assembly. Since its inception, much has changed. Today's highly dense printed circuit boards shorten the conductive pathways, require far different material sets, and problematic residues are site-specific. For many of today's PCBs, the ROSE bulk extraction method provides limited information as to acceptable and unacceptable cleanliness across an entire assembly.

In 2015, the IPC J-STD-001 committee assigned a team to develop the next generation of "cleanliness" requirements[1]. The project objectives were as follows:

- Proposed re-write of Section 8 for committee review
- Generate an associated white paper to explain the new section to stakeholders
  - Need to address: clean and no-clean processes, process validation, and process monitoring
  - What does the "next generation" of ionic residue testing/validation look like?

J-STD-001G, Amendment 1 standard defines a Qualified Manufacturing Process (QMP)[2].

*Unless otherwise specified by the User, the Manufacturer **shall [N1D2D3]** qualify soldering and/or cleaning processes that result in acceptable levels of flux and other residues.Objective evidence **shall [N1D2D3]** be available for review. Rework processes **shall [N1D2D3]** be included in the process qualification.*

The use of the 1.56 µg/NaCl equivalence/cm2 value for ROSE (Resistivity of Solvent Extract), with no other supporting objective evidence, is not considered an acceptable basis for qualifying a manufacturing process.

A Qualified Manufacturing Process should be determined using some form of temperature-humidity-bias sort of testing (such as SIR). Qualifying a manufacturing process through chemical analysis alone (e.g. ion chromatography) does not tell you the effects of the residue under humid conditions, which is where electrochemical failures occur. Companies that have come up with ionic standards by IC usually had temperature-humidity-bias (THB) testing somewhere in the background.

Temperature-Humidity-Bias (THB) Testing

THB testing is done to show evidence of the loss of integrity or reliability in the material system used to assemble the printed circuit board[3]. Loss of integrity may include conformal coating or solder mask adhesion failure (less protection from the environment), decreases in dielectric strength, electrolytic corrosion, or electrochemical migration. Each of these may represent shortcomings in materials, manufacturing methods, or a susceptibility to a particular failure mechanism, which would not be desirable in the end product.

This testing regime subjects a material or material system to a specific duration of temperature and humidity higher than ambient conditions. The oxygen barriers (rosin) in flux residue, softens when exposed to elevated temperatures. The ionic residues present on the assembly dissolve in moisture (relative humidity). The acidic nature of these ionic residues reacts with metal oxides present in the residue field. When an electrical potential is applied between adjacent electrodes, the metal ions will be attracted to the cathode. Electrolytic corrosion and electrochemical migration result.

Figure 1 illustrates the chemical complexity of flux residue[4]. These residues can vary based on melting temperature, complexation, redox, dissolution, decomposition, and vaporization. The chemical equilibria are strongly affected by the reflow profile and atmosphere. When running a no-clean process, it is critical to select a solder paste where the activators outgas and decompose at the thermal profile and reflow environment. Leadless and bottom terminated components can block outgassing channels, which results in an active residue.

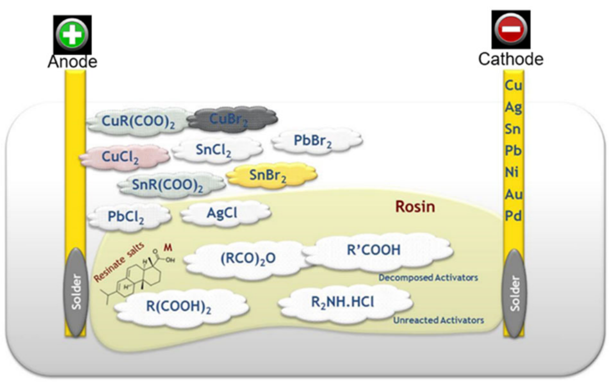


Figure 1: Flux Residue Interactions

IPC TM-650 2.6.3.7 method tests the material system at 40°C, 90% RH, for 168 hours[5]. At these conditions, no-clean flux residues begin to volatilize. The reason for the 40 °C, 90% RH method is because most no-clean flux residues begin to volatilize at this temperature. The residues on the surface can contribute to electronic failures. This test regime artificially ages a materials system, simulating years of service by days of testing. This test method helps reliability engineers gain an estimate of the long-term service life.

Harsh Climatic Conditions

Electronic products are used in varying climatic conditions. Highly dense assemblies comprise a large population of leadless and bottom terminated components. Changes from the external climatic conditions can cause uncontrolled moisture inside the device enclosure[6]. Uncontrolled humidity, together with other factors, introduces deviation from desired functionality resulting in intermittent or permanent failure of the device.

The materials that make up the printed circuit board, components, and conformal coating influence moisture absorption when exposed to climatic conditions[6]. Miniaturization, leadless components, and conductor pitch result in closer distance between biased points on the PCB. These increases in the electric field combined with tighter pitch create a higher potential for leakage currents and electrochemical migration.

Ionic contaminants dissolved in the water film is referred to as an electrolyte. The residue field influences the electrical property of the water film. The water film thickness depends on the humidity, temperature, and hygroscopic residues present on the PCB. Failure is dependent by the interplay of these electrochemical sequences resulting in a parasitic circuit of different capacity that interferes with the electrical aspects of the PCB. When this electrolyte connects the conductors, the metal cations form dendrites that migrate and plate onto the insulating solder mask.

Corrosion reliability of electronic devices can be increased by optimizing processes, materials, component designs, PCB, and enclosure design. The reliability of the PCB encompasses each of these conditions, which include cleanliness. Temperature-humidity-bias testing is the best method for determining the robustness of each of these factors. The test medium that integrates these test conditions is known as Surface Insulation Test Method.

Surface Insulation Resistance (SIR)

SIR is a property of the material and electrode system. The test measures the electrical resistance between two electrical conductors separated by a dielectric material. SIR detects bulk conductivity, leakage through electrolytic contaminants, and metallization integrity.

The origins of SIR testing focused on characterizing materials. As electronics evolved from thru-hole to surface mount connections, advances in test boards opened this test methodology to process characterization. The potential applied between adjacent connectors of a test pattern determines the surface resistance. As such, SIR is the best test method for determining the corrosive potential of process residues present on the surface and adjacent to conductors.

Figure 2 illustrates the SIR test method.

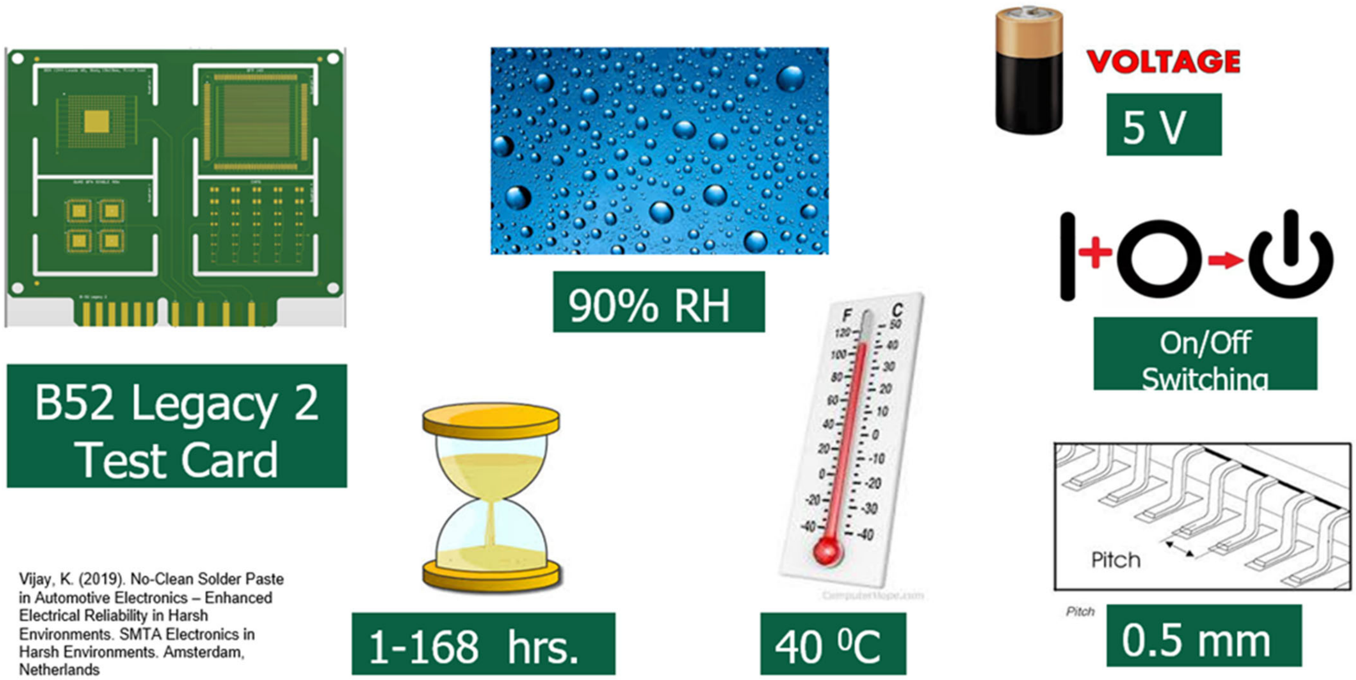


Figure 2: SIR Test Method

Figure 3 highlights process areas where SIR testing can be applied. A series of designed experiments using the SIR method were studied.

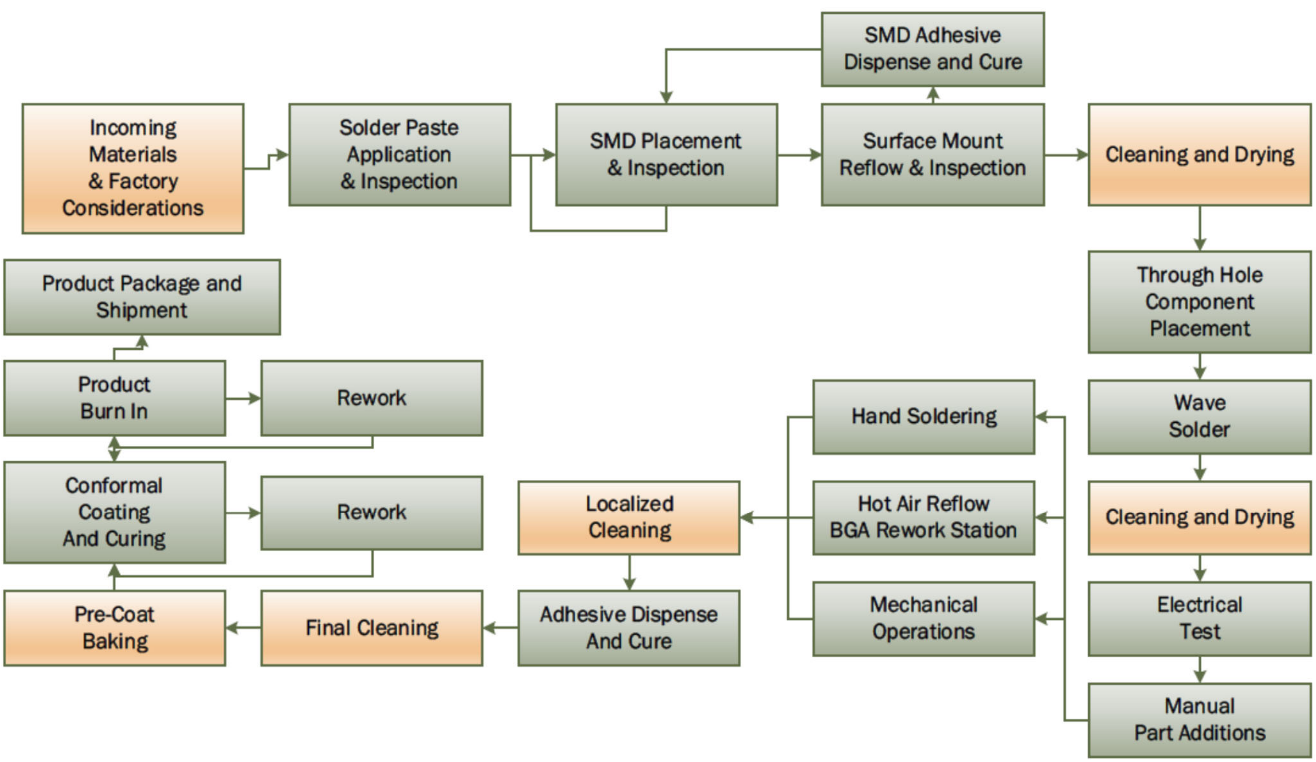


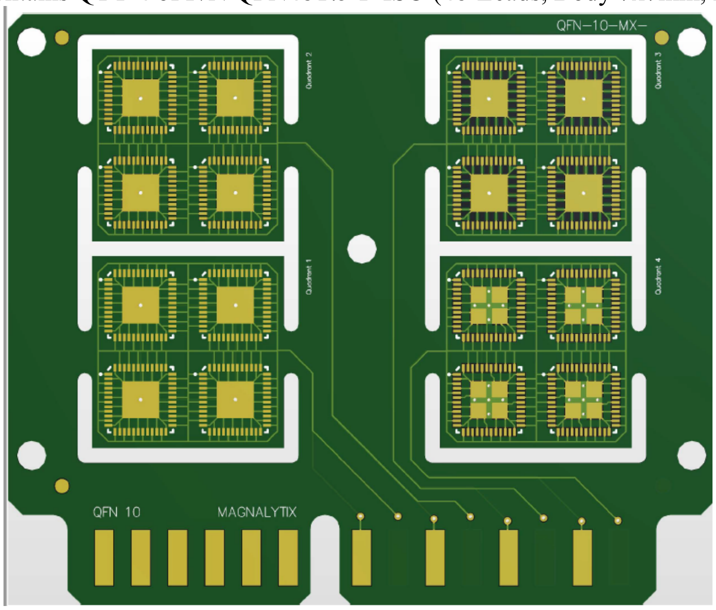
Figure 3: Process Areas where SIR Testing can be to Determine Residue Impacts[1]

Experimental

DOE 1: Bottom Terminated Component

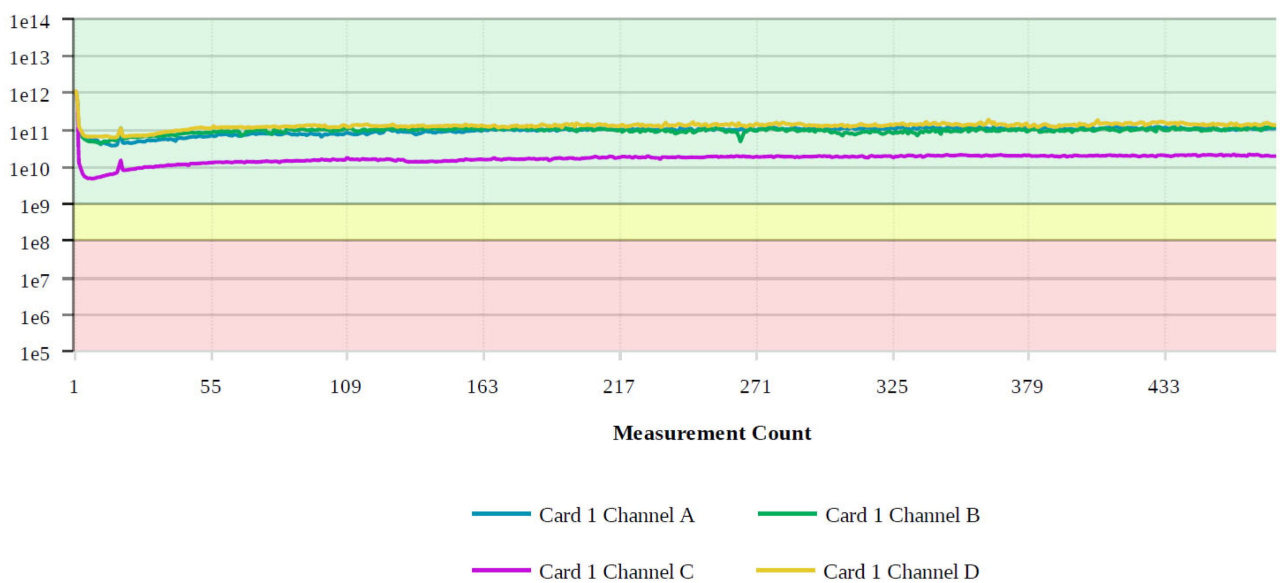
Characterization of a low residue No-Clean solder paste was evaluated using a SIR test board. Solder Mask design patterns across four quadrants allow for the study of flux activator outgassing and decomposition.

- QUADRANT 1 - Contains QTY 4 of P/N QFN48T.5-F-ISO (48-Leads, Body 7x7mm, Pitch 0.5mm)
- QUADRANT 2 - Contains QTY 4 of P/N QFN48T.5-F-ISO (48-Leads, Body 7x7mm, Pitch 0.5mm)
- QUADRANT 3 - Contains QTY 4 of P/N QFN48T.5-F-ISO (48-Leads, Body 7x7mm, Pitch 0.5mm)
- QUADRANT 4 - Contains QTY 4 of P/N QFN48T.5-F-ISO (48-Leads, Body 7x7mm, Pitch 0.5mm)

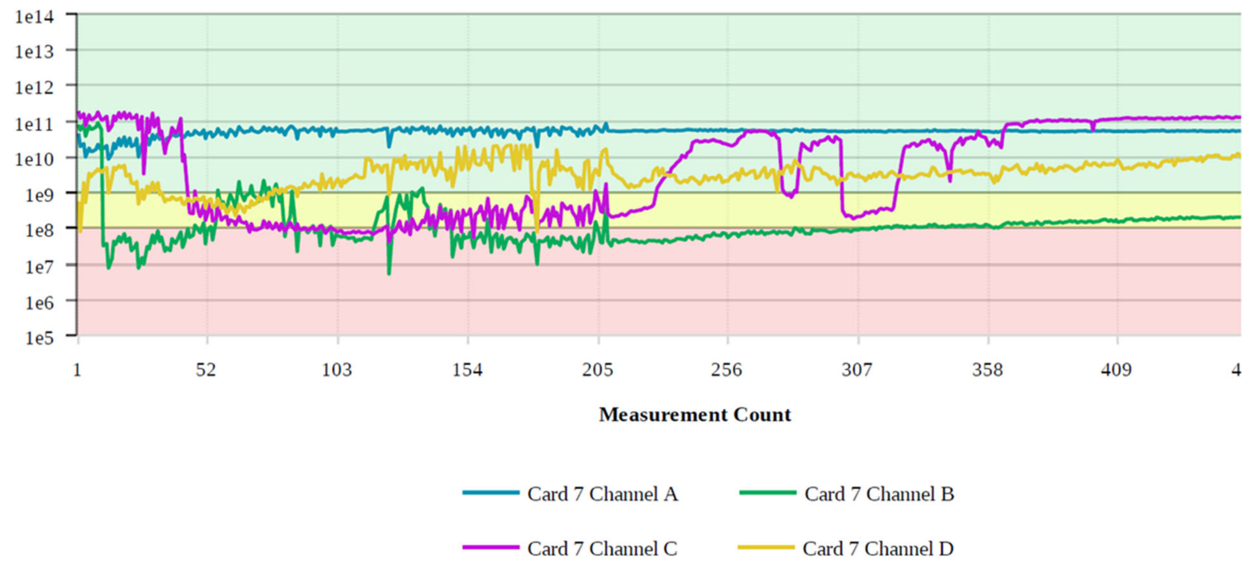


Three cleaning conditions were tested:

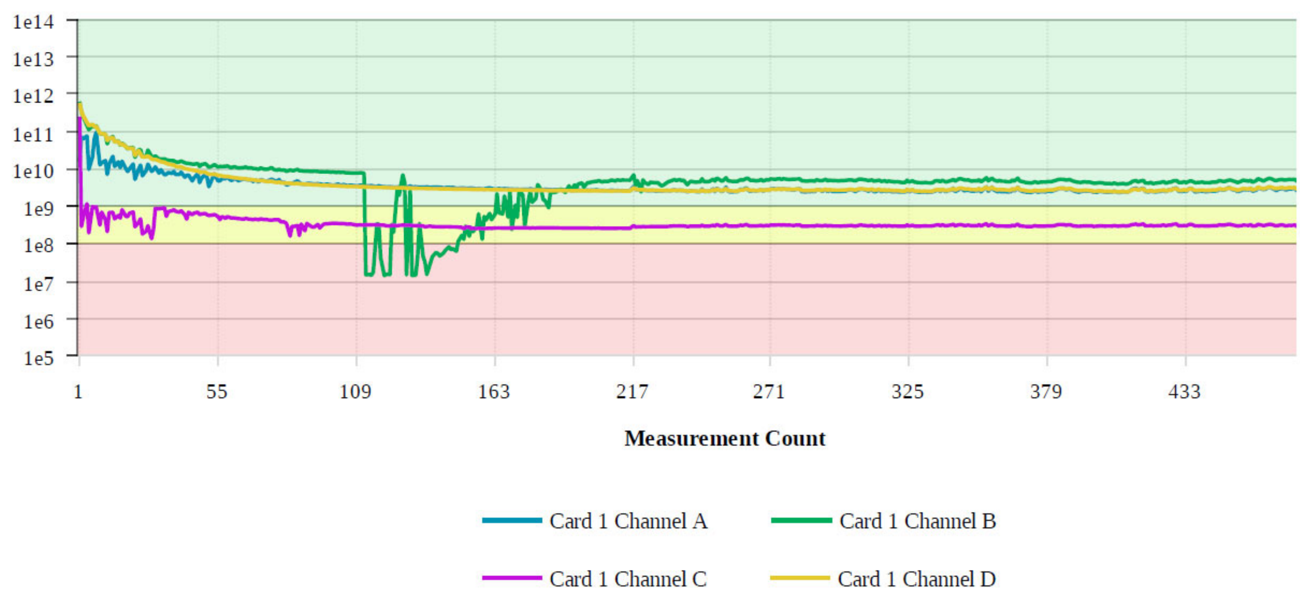
- Cleaned Condition: All four quadrants were reliable



- Partially Clean Condition: Residue present under the components showed activity when tested under temperature-humidity-bias testing



- Non-Cleaned Condition: Three channels passed SIR but with lower values than the cleaned condition

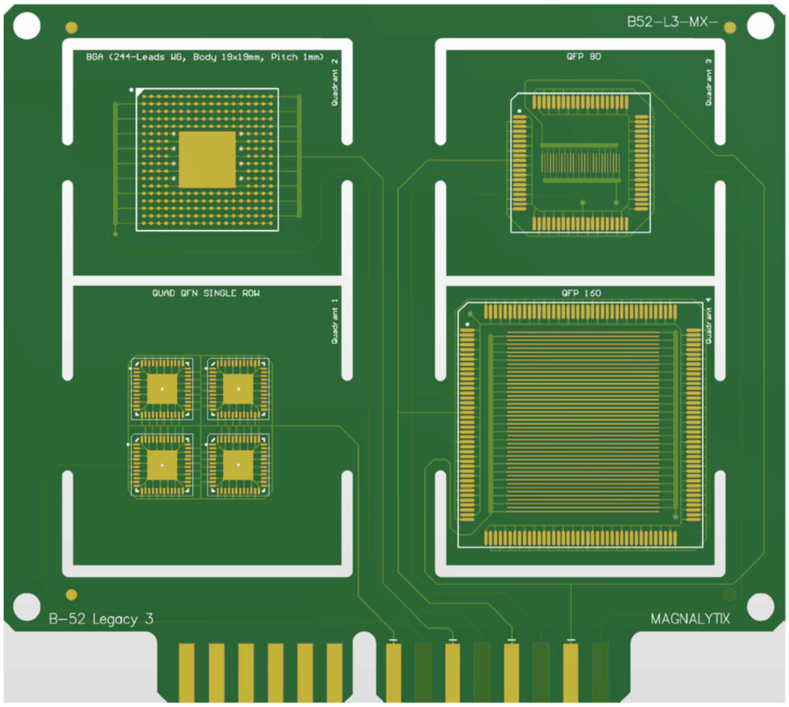


The SIR test methodology was effective at characterizing the activity of a low residue no-clean flux residue. The SIR traces measured surface insulation resistance of conductors between pin-to-pin and pin-to-thermal lug. Cleaning the flux residue under the component termination resulted in high surface insulation resistance. A partial clean condition showed a far different result to that of a cleaned part. The activity of the residue left under the component termination indicates a high risk of electrochemical migration when operated in a harsh environment. The SIR values for the No-Clean condition were lower than the clean condition but better than a partially clean condition. Patterning solder mask windows with thermal vias was the most stable condition for designing for a No-Clean process.

DOE #2: Characterizing Residue Effects across Four Component Designs

Four component designs were patterned onto this SIR Test Board.

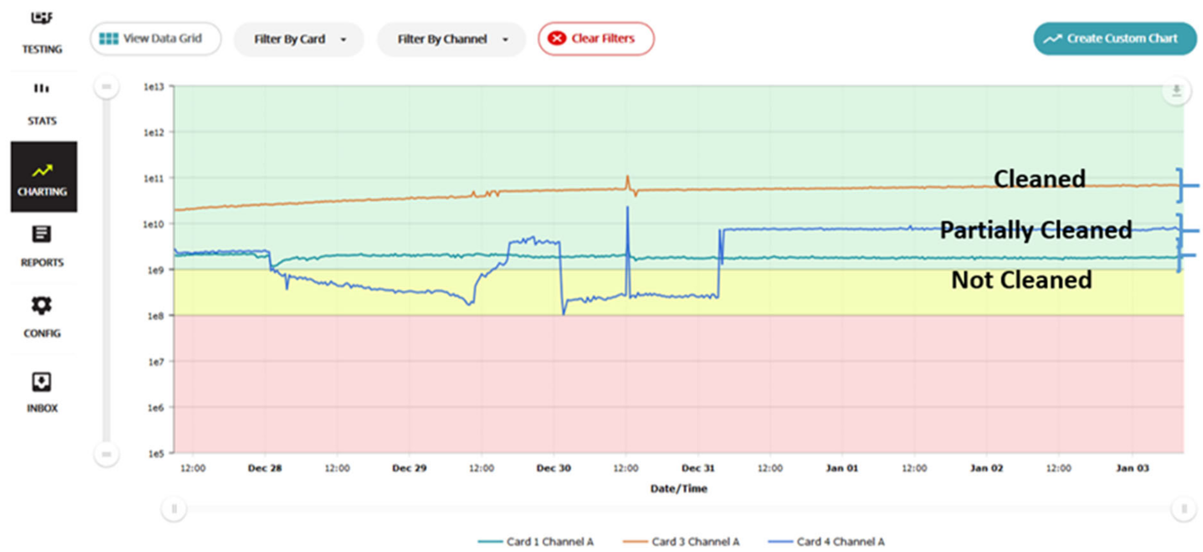
QUADRANT 1 - Contains QTY 4 of P/N QFN48T.5-F-ISO (48-Leads, Body 7x7mm, Pitch 0.5mm)
QUADRANT 2 - Contains QTY 1 of P/N FBGA 244 (244-Leads WG, Body 19x19mm, Pitch 1mm)
QUADRANT 3 - Contains QTY 1 of P/N QFP80 (80-Leads, Body 14x14mm, Pitch 0.65mm)
QUADRANT 4 - Contains QTY 1 of P/N QFP160 (160-Leads, Body 28x28mm, Pitch 0.65mm)



Factors investigated:

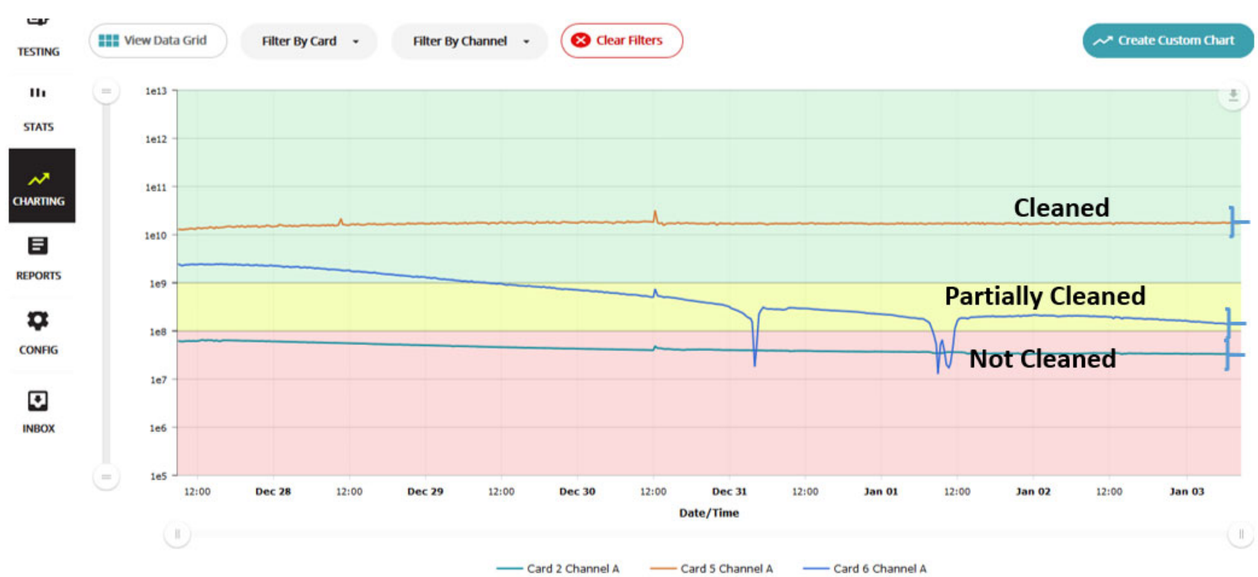
- Aqueous cleaning material
  - Concentration: 15%
  - Upper Wash Pressure: 80 psi
  - Lower Wash Pressure: 60 psi
  - Upper Rinse Pressure: 60 psi
  - Lower Rinse Pressure: 40 psi
- No Clean Solder Paste
  - SnPb Solder Paste #1
  - SnPb Solder Paste #2
  - Pb-Free Solder Paste #3
- Cleanliness
  - Not cleaned
  - Inline Cleaning Machine with a Belt speed: 1 FPM
  - Inline Cleaning Machine with a Belt speed: 2 FPM
- SIR (IPC-TM-2.6.3.7)
  - Voltage Bias: 8 volts
  - Temperature: 40°C
  - Relative Humidity: 90%
  - Time: 168 Hours

Solder Paste # 1: QFN Net



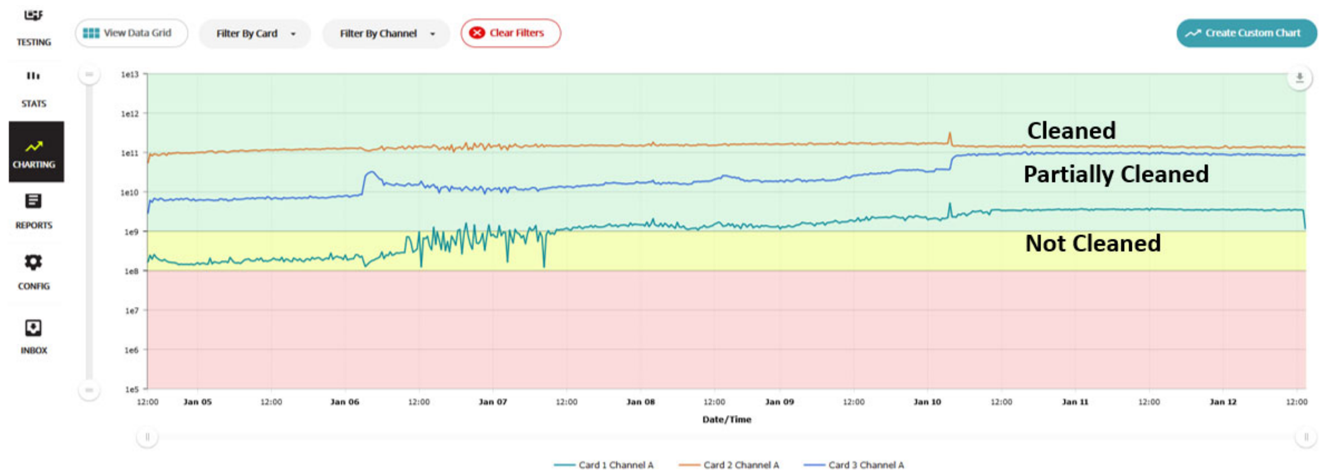
The QFN bottom terminated component is a challenging component due to the low standoff and high thermal mass of solder. When the QFN is cleaned, the SIR values are over 2 decades higher. The concern is when errant residue is still present under the QFN post cleaning. The SIR values indicate that the residues are active. Dialing in the cleaning process to assure that the QFN is cleaned is an important criteria.

Solder Paste #2: QFN Net



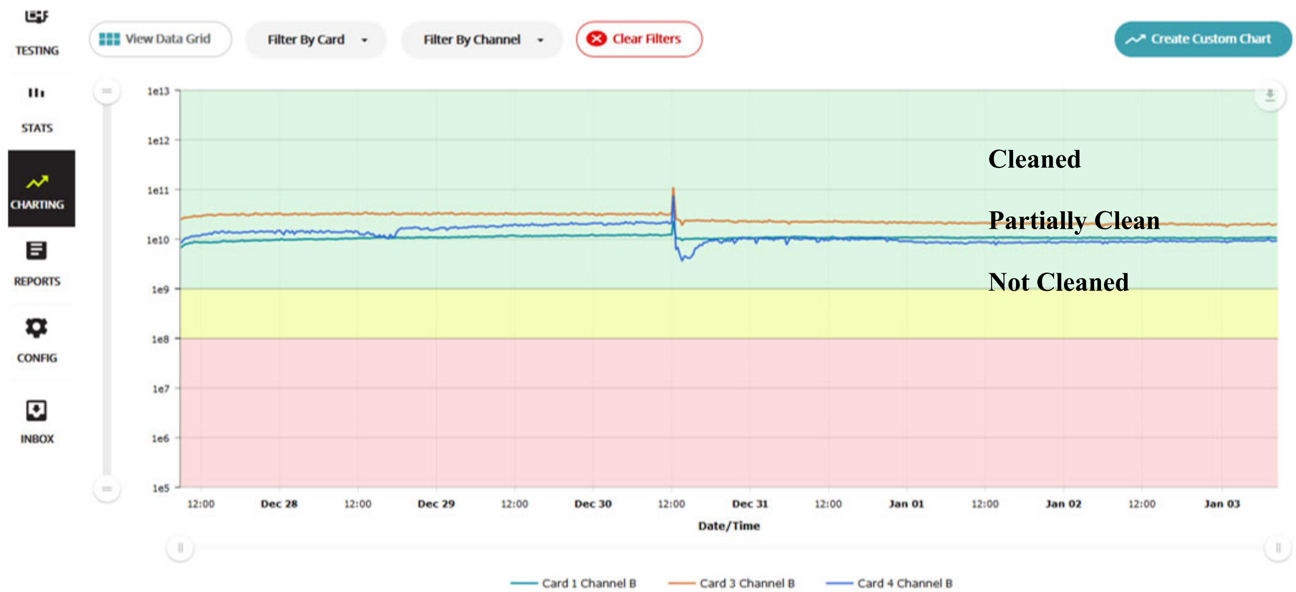
On solder paste #2, the activity level of this paste is apparent. If cleaned, the SIR values meet the desired criteria. If residue is left under the bottom termination post cleaning, the SIR values move into the danger zone.

Solder Paste # 3: QFN Net



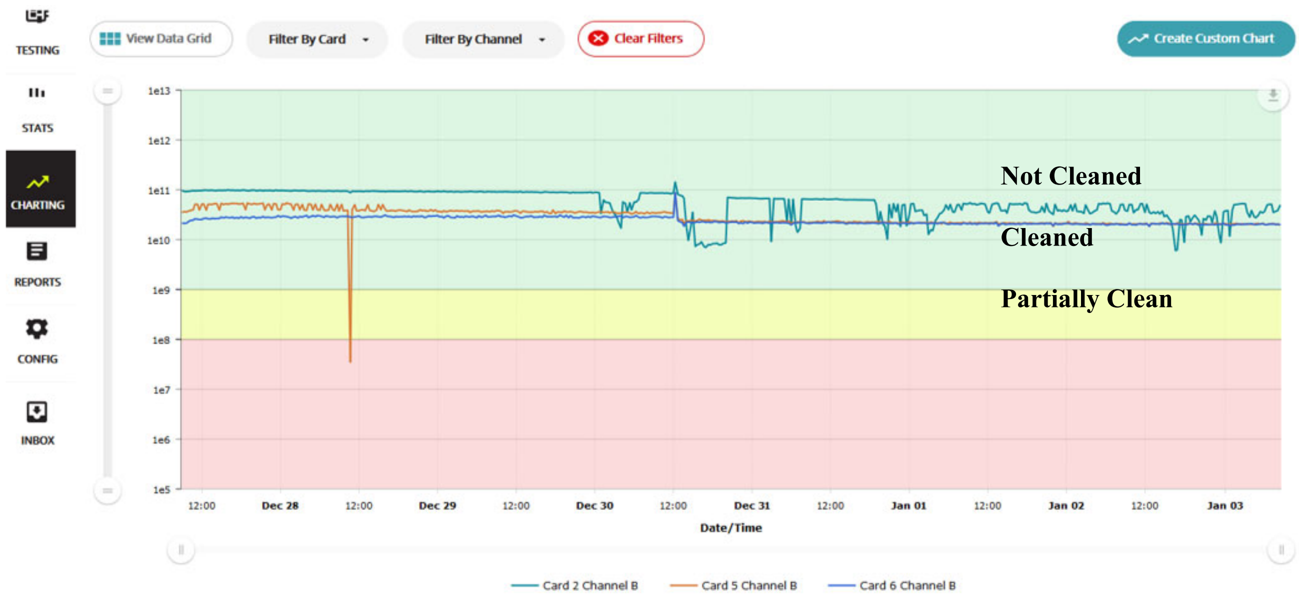
This Pb-Free solder paste showed a benign residue condition.

Solder Paste #1: BGA



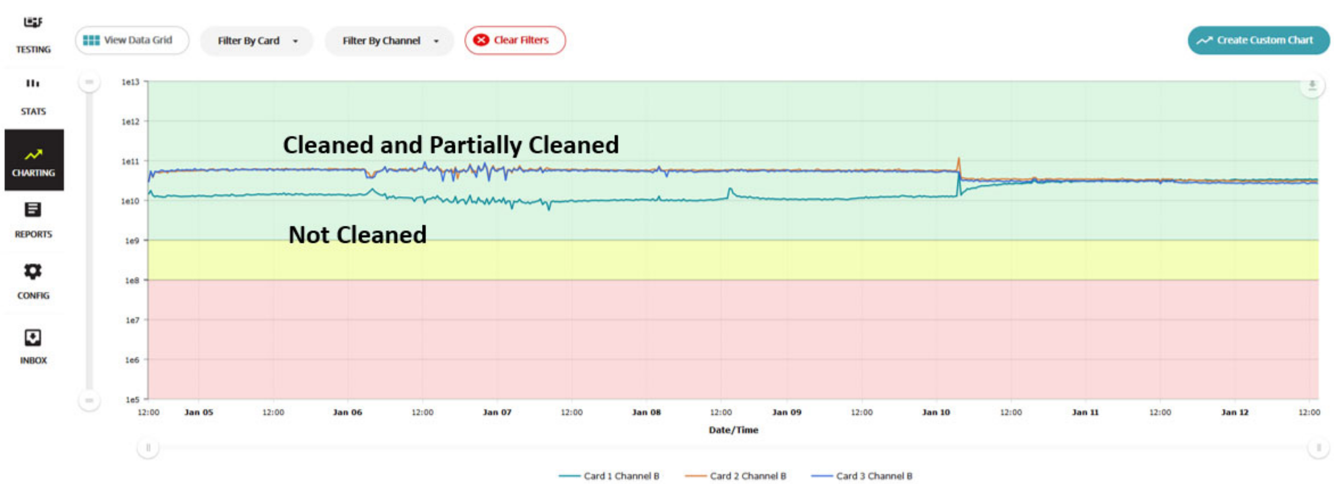
Notice the consistency of the FBGA component. The high standoff of roughly 254µms provides good outgassing. The part is easily cleaned, resulting in SIR values in the desired range. Even for Not Cleaned boards, the SIR values are excellent.

Solder Paste #2: BGA



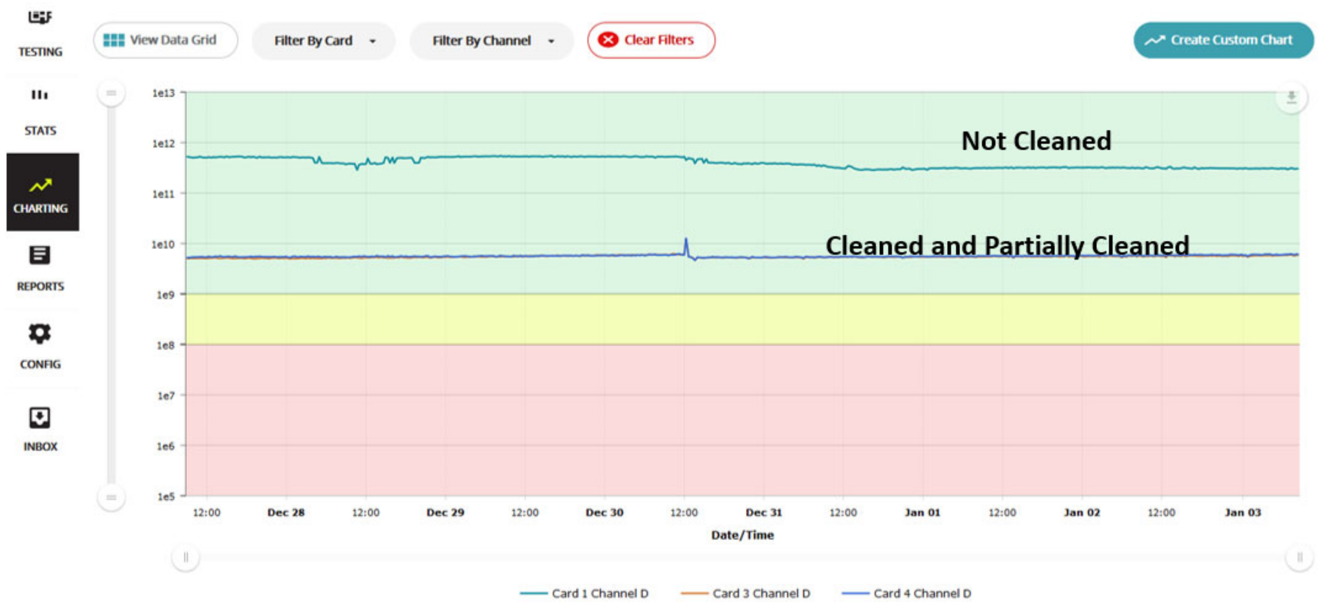
For solder paste #2, there is evidence of a leakage current event on the partially cleaned board, but with full recovery. The SIR values all range in the desired zone.

Solder Paste #3: BGA



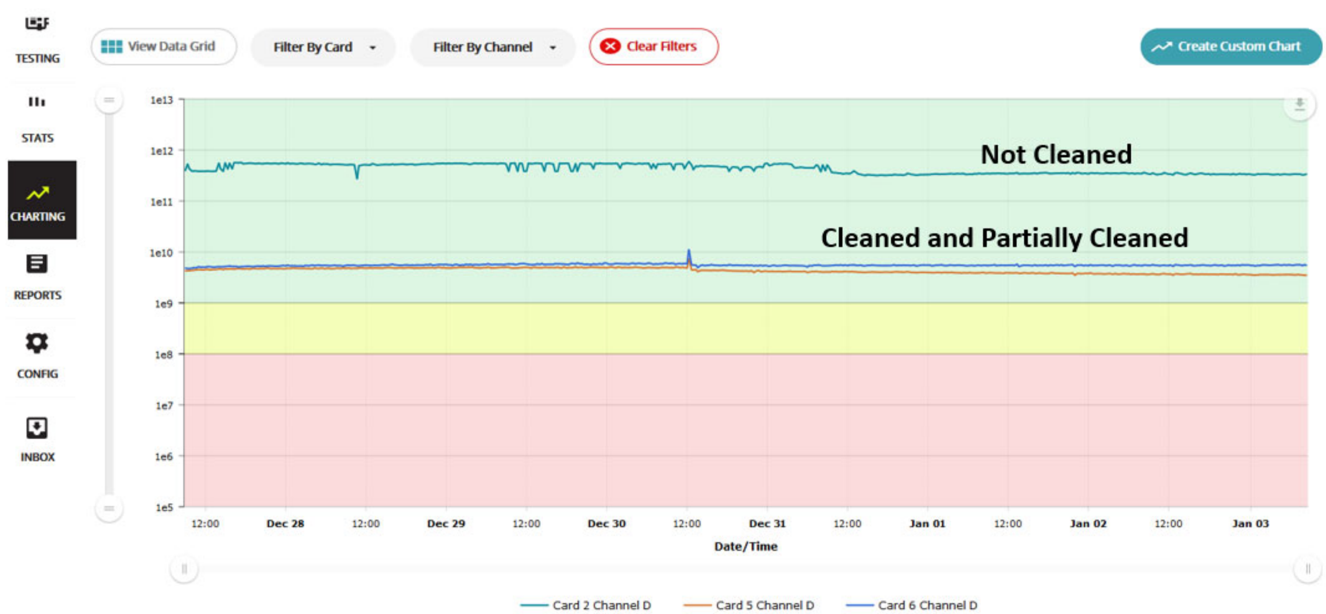
The Pb-Free solder paste #3 shows consistency on the FBGA regardless of the cleaning condition.

Solder Paste #1: QFP 160



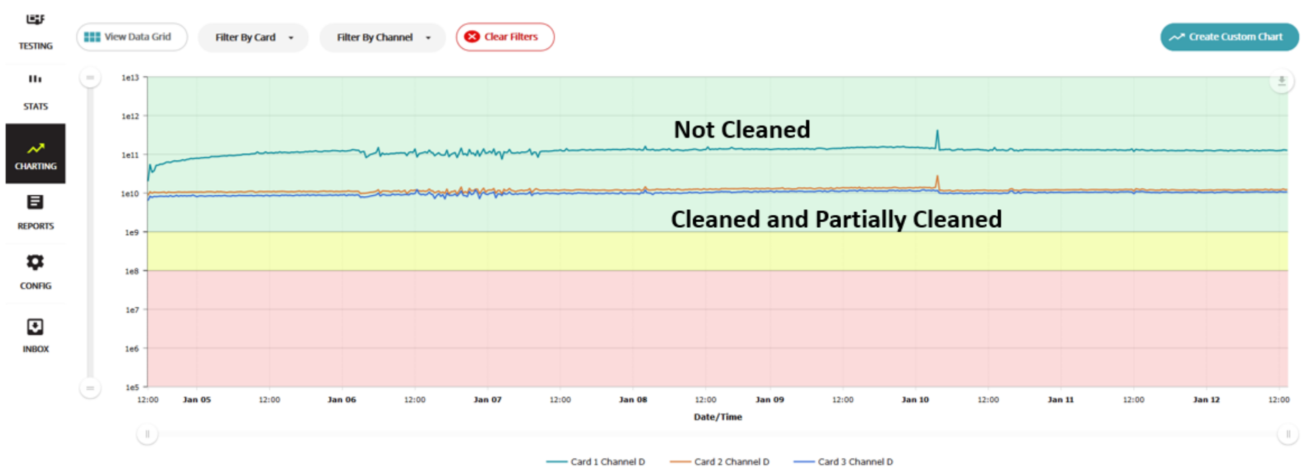
The QFP is a leaded component. When the flux component sees proper heat transfer and outgassing during reflow, the not cleaned residue is highly reliable. Both cleaned and partially cleaned residues were lower than the no-cleaned residue but still reliable.

Solder Paste #2: QFP 160



On the higher activity solder paste #2, the behavior on the QFP is similar to solder paste #1.

Solder Paste # 3: QFP 160

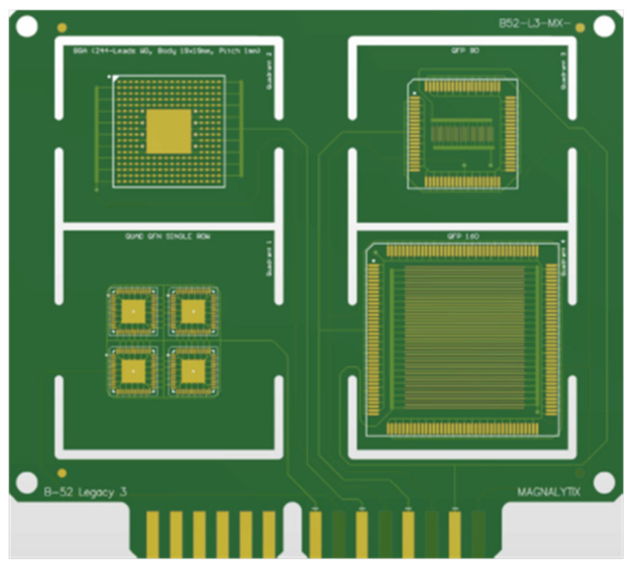


The data indicate that reliability varies from component to component. For the QFP160, the flux is benign due to activator outgassing and decomposition.

DOE 3: Batch Cleaning Study

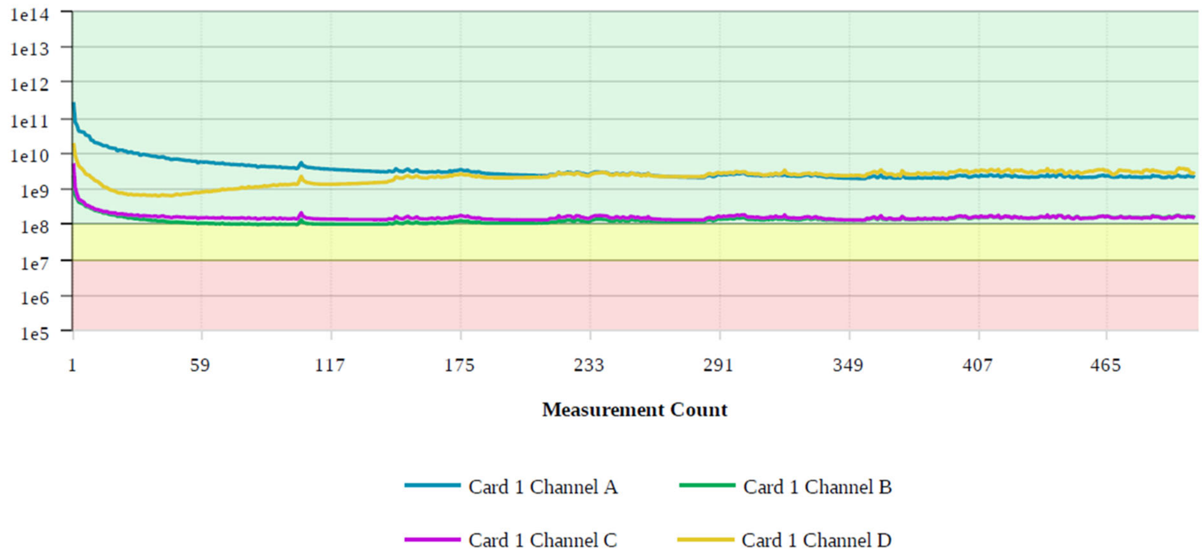
The purpose of this DOE is to evaluate new cleaning agents in a cabinet style batch cleaning tool.

- Aqueous cleaning material
  - Cleaning Agent #1 @ 15%
- No Clean Solder Paste
  - SnPb Solder Paste #1
  - SnPb Solder Paste #2
- Wash Temperature
  - 55°C
  - 60°C
- Wash Time
  - 15 Minutes
- Cleaning Machine
  - Cabinet style batch cleaning machine
- Rinse
  - 500 kΩ
- SIR Test Board



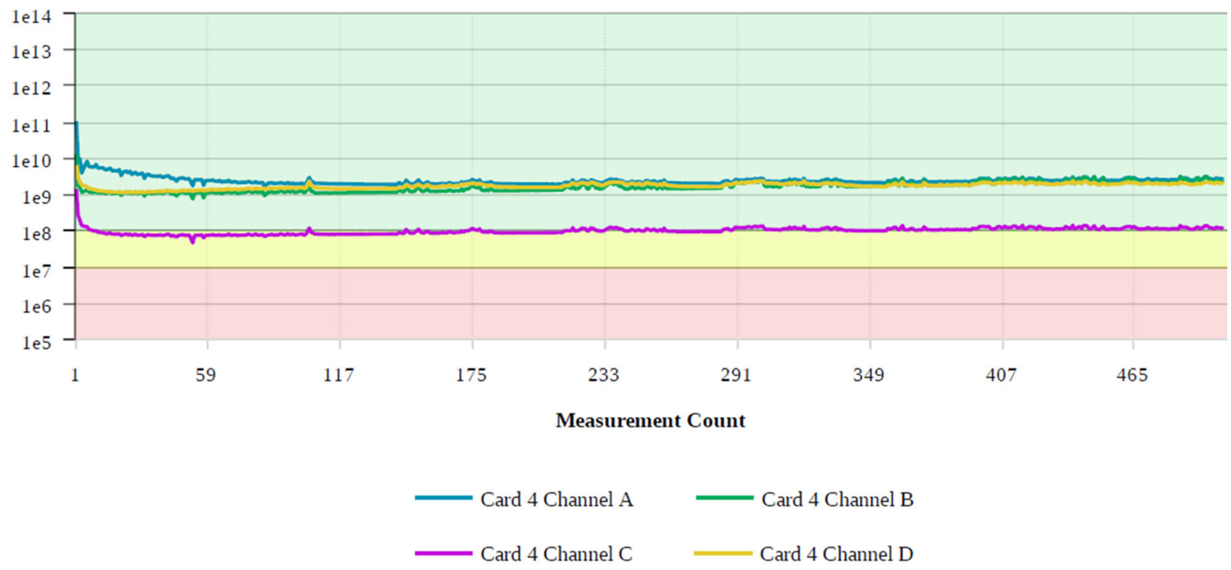
New Cleaning Agent

- Solder Paste # 1
- 55°C



New Cleaning Agent

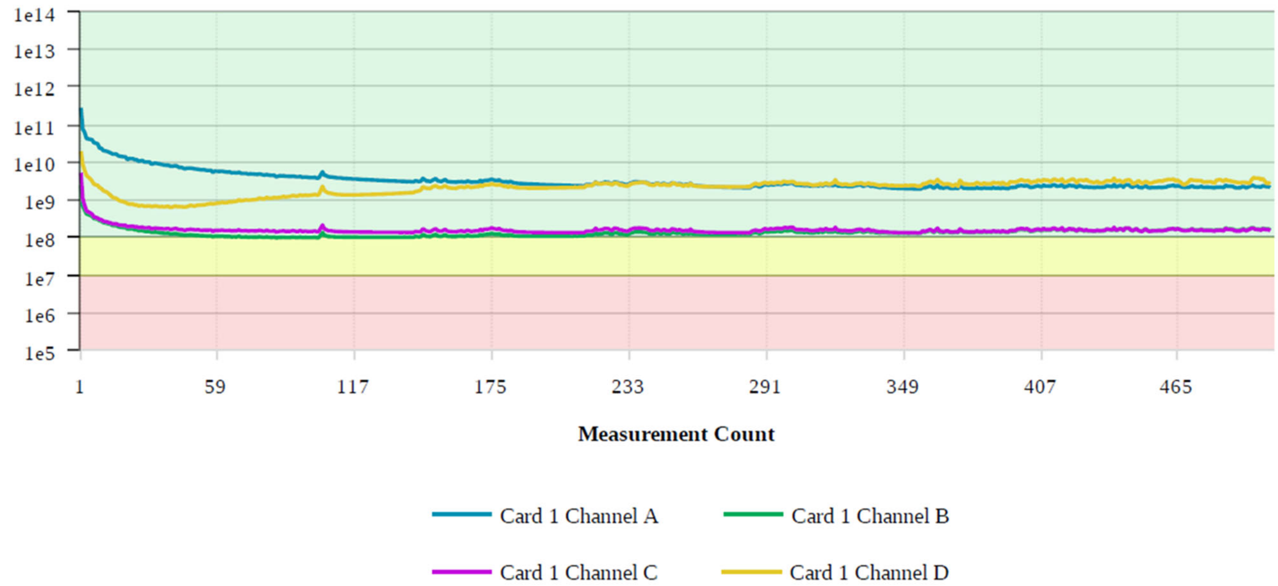
- Solder Paste # 1
- 60°C



Increasing wash temperature to 60°C improved performance on the QFN component. For both wash temperatures, the QFP80 was at least 1 decade lower. This component is excellent for measuring rinse performance since the SIR comb pattern is under the component body. Setting the rinse water resistivity to 250 kΩ instead of 500 kΩ would most likely improve this condition.

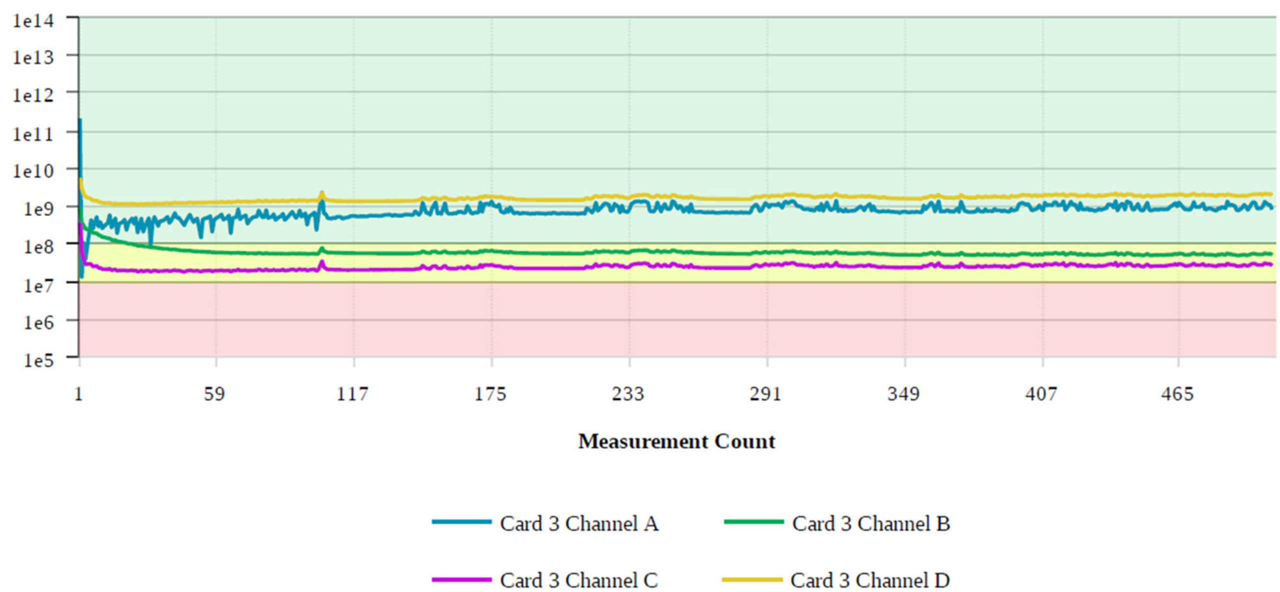
New Cleaning Agent

- Solder Paste # 2
- 55°C



New Cleaning Agent

- Solder Paste # 2
- 60°C

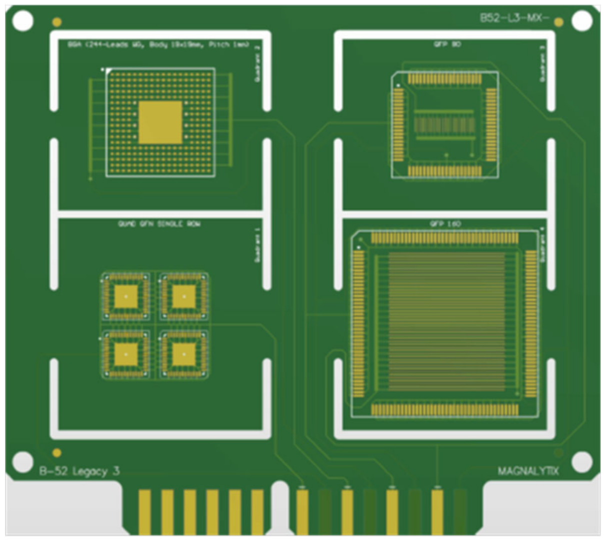


Both solder pastes performace similiarly. Increasing temperature to 60°C improved cleaning performance on difficult to clean QFN and QFP 80 components

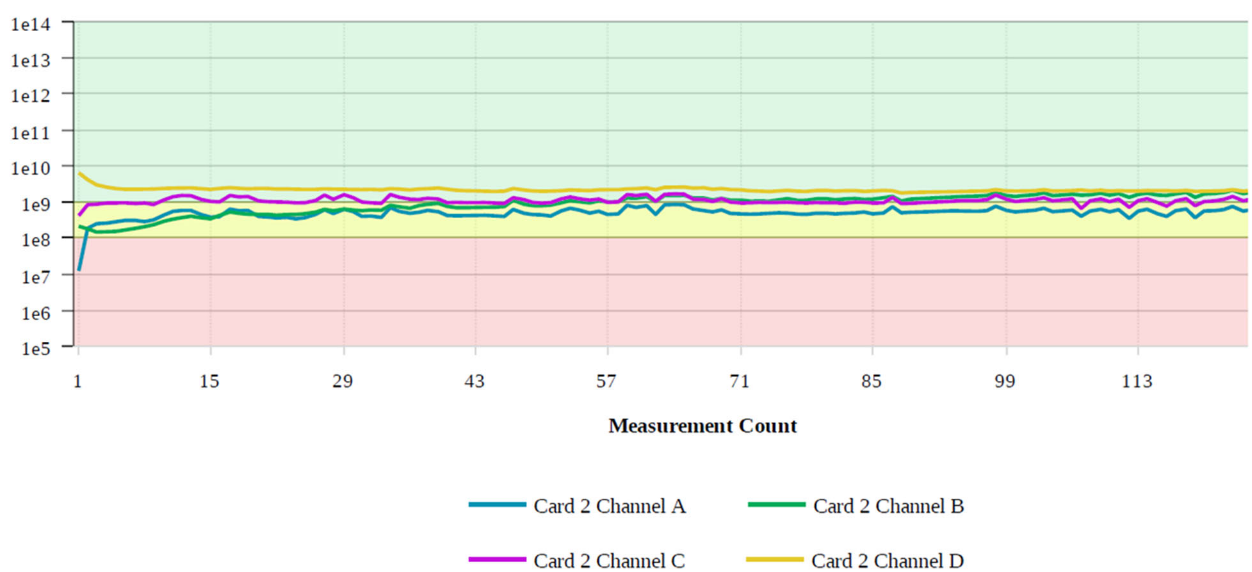
DOE 4: Inline Cleaning Agent Rinsing Study

The purpose of this DOE was to determine rinse performance as a function of belt speed using an inline cleaning machine.

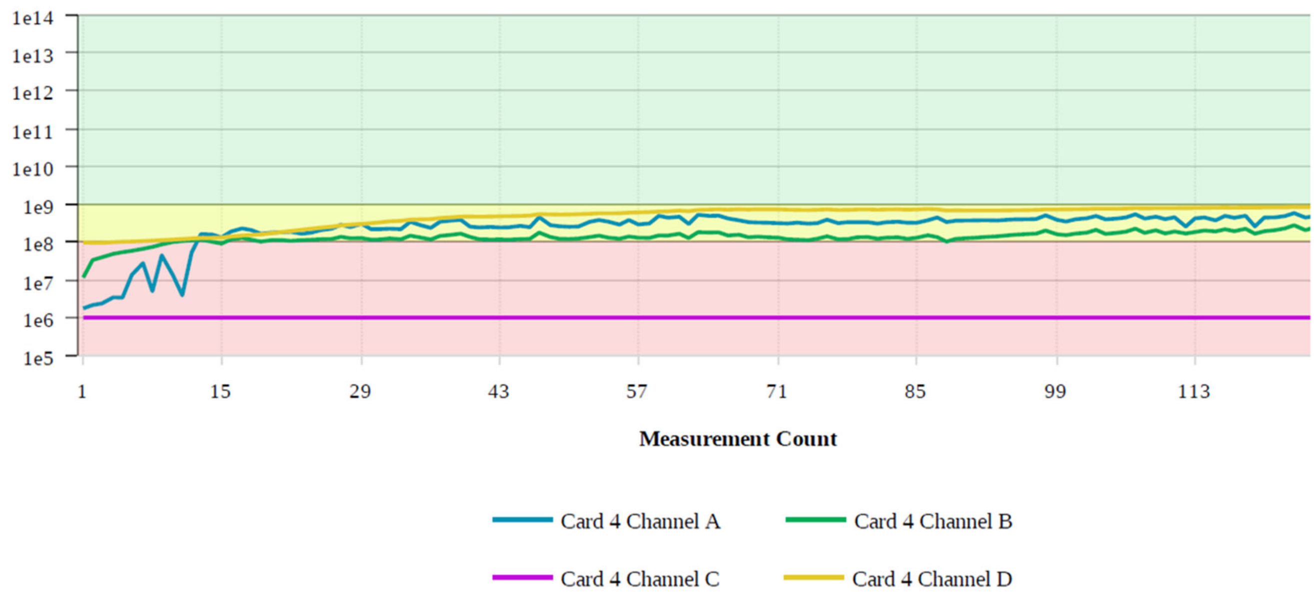
- SIR Test Board
  - Boards Cleaned before running test
  - SIR values exceed 10 log Ω for each channel before running the test
- Belt Speed
  - 0.5 feet/minute
  - 1.5 feet/minute
  - 3.0 feet/minute
- Rinse Temperature
  - 60°C



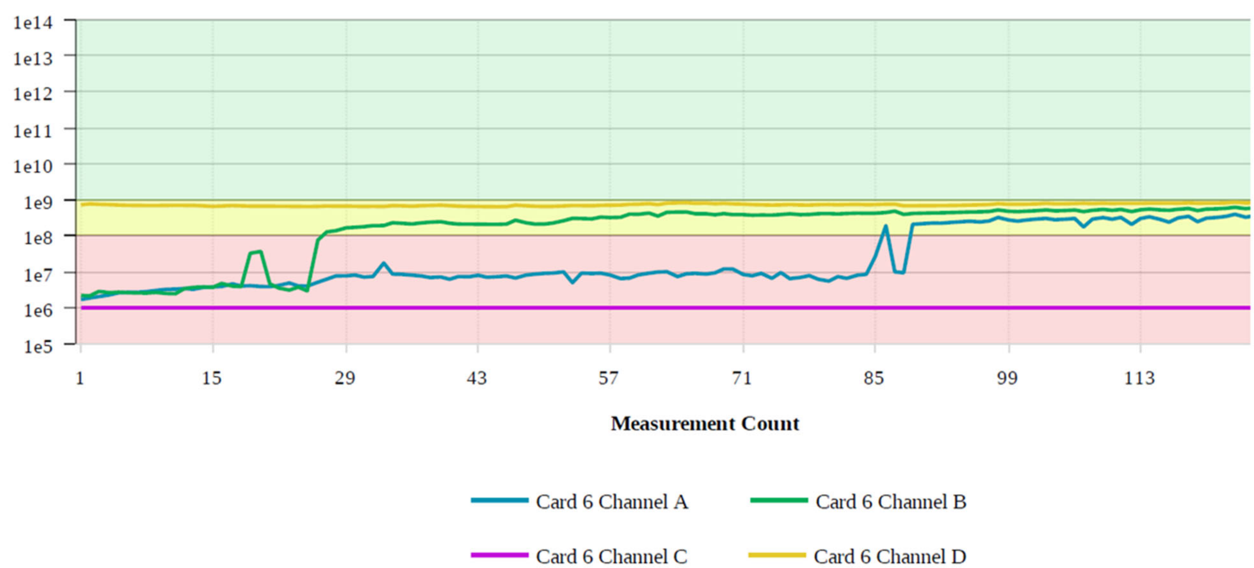
Belt Speed ~ 0.5 feet/minute



Belt Speed ~ 1.5 feet/minute



Belt Speed ~ 3.0 feet/minute



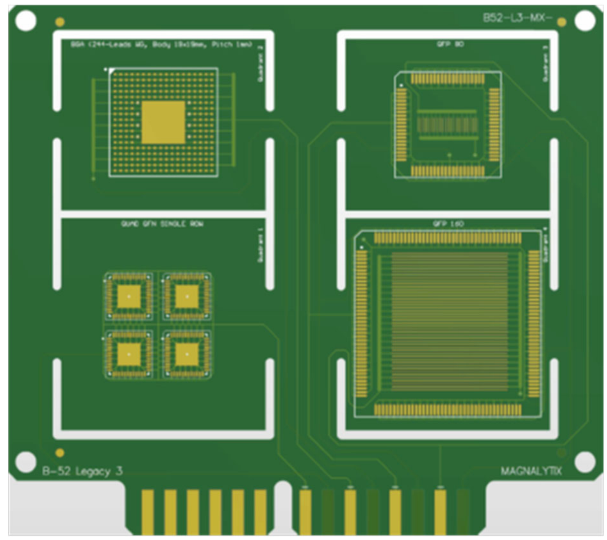
SIR method is effective at studying rinsing effects on specific components. Lower resistivity values on specific components declined with faster belt speeds. This type of study can be useful for setting process parameters. Channel C (QFP 80) device shorted due to a bridge between two pins.

DOE 5: Bath Life Study

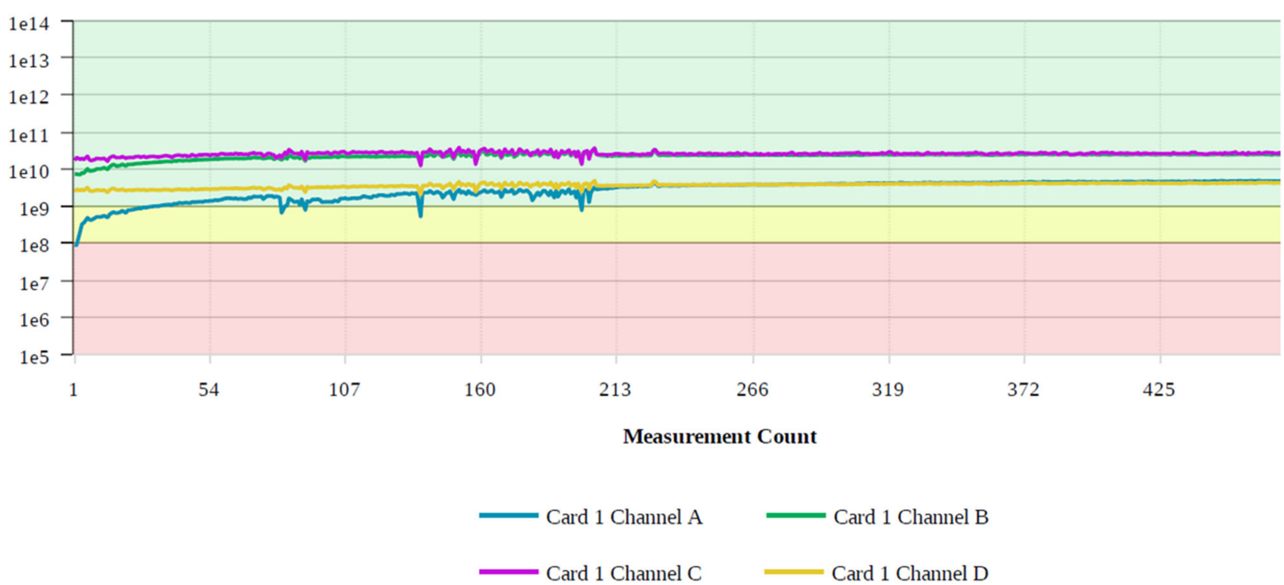
Aqueous cleaning agents are common for cleaning printed circuit boards following the soldering process. Flux residues accumulation into the wash bath will eventually load the wash bath with non-volatile residue. As the wash bath loads, cleaning and rinsing performance can decline.

The purpose of this DOE is to monitor wash bath life over time.

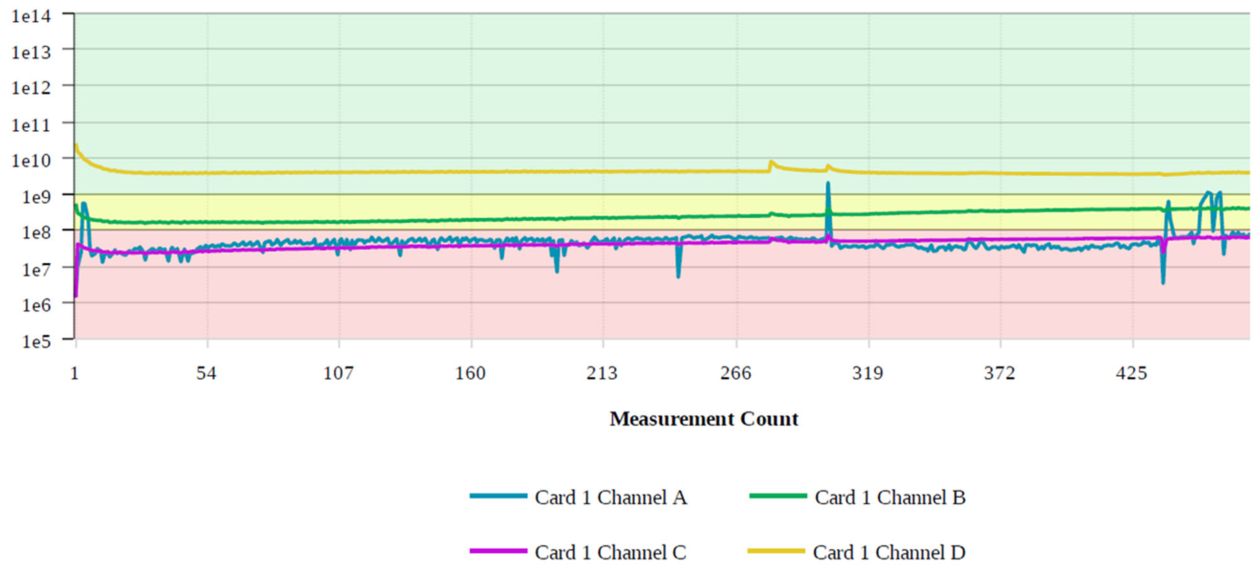
- SIR Test Board
- Aqueous Cleaning Bath
    - Week 1: Fresh Charge
    - Week 6: Aged Bath
- Wash Temperature
    - 65°C
- Rinse Temperature
    - 60°C
- Solder Paste
    - SAC 305



Week 1: Fresh Charge



Week 6: Aged Wash Bath



Similar to the rinsing study, SIR method is effective at bath aging. Lower resistivity values on specific components declined as the wash bath loads. This type of research can be useful for determining the life of the wash bath as well as changes in cleaning performance.

Inferences from Data Findings

Reliability is the ability of a product to properly function, within specified performance limits, for a specified period, under the life cycle application conditions[7]. Test boards populated with components and routed with sensor traces that impart process information help to assure that the process used to build production hardware is reliable. The SIR test method has a long history of use for characterizing materials and processes but has not found use at the assembly site.

The research presented in this paper illustrates the power of the SIR method at the assembly site. The tool finds application in system design, characterizing the process, controlling the process, and quality assurance. The tool allows engineers to track process conditions, and to determine reliability chemically when exposed to environmental conditions.

CONCLUSIONS

When a product fails, there are costs. To the manufacturer, these costs include time-to-market increases, warranty costs, and decreases in market share. Failures can stain the reputation of a company and deter new customers. Claims for damages caused by product failure is an inconvenience to your customer; resulting in personal injury; loss of mission; service or capacity; cost of repair or replacement; and result in indirect costs, such as an increase in insurance, damage to reputation and loss of market.

The common practices to requalify a process occurs when changing flux bearing materials, cleaning agents, supplier changes, and geographic changes. Electrical testing uses the SIR method for requalification testing. Once a process is qualified, ROSE testing has been the method of choice for monitoring and controlling the process. The ROSE method is only an indicator. Conversely, the SIR method provides quantitative information as to the presence of residues, and their impact on the reliability. The SIR method provides assurance that the process qualified at the inception is still in control. The method can be used to determine the activity of residues trapped under leadless and bottom terminated components, flux bearing material differences, cleaning materials, cleaning machines, rinsing effectiveness, and bath life.

REFERENCES

1. Pauls, D. (2017, August). Wisdom Wednesday – The proposed Section 8 Cleanliness for J-STD-001. IPC, Bannockburn, IL.
2. IPC-WP-019. (2017, August). An Overview of Global Change in Ionic Cleanliness Requirements. IPC, Bannockburn, IL.
3. IPC 9201A. (2007). Surface Insulation Resistance Handbook. IPC, Bannockburn, IL.
4. Tolla, B. (2017). Impact of reflow and cleaning processes on the electrochemical activity of flux residues. SMTA-SMART Group Cleaning and Coating Conference. Amsterdam, Netherlands. SMTA, Minneapolis, MN.
5. IPC-TM-650, 2.6.3.7. (2007). Surface Insulation Resistance. IPC, Bannockburn, IL.

6. Ambat, R. (2019). Water Film Formation on PCBA Surface and Humidity Robustness of Electronics. Univerity of Denmark. SMTA Harsh Environments Conference. Amsterdam, Netherlands.
7. Sood, B. (2019). Focus on PCB Reliability to Drive Quality. IPC Reliability Forum. Baltimore, Maryland. IPC, Bannockburn, IL.
8. Karthik, V. (2019). No-Clean Solder Paste in Automotive Electronics – Enhanced Electrical Reliability in Harsh Environments. SMTA Electronics in Harsh Environments, Amsterdam, Netherlands. SMTA, Minneapolis, MN.

AUTHORS

Dr. Mike Bixenman
Co-Inventor
Magnalytix
mbixenman@magnalytix.com

Chief Technology Officer
KYZEN Corporation
Nashville, TN, USA
mikeb@kyzen.com

Mark McMeen
Co-Inventor
Magnalytix
mmcmeen@magnalytix.com

Vice President
STI Electronics
Huntsville, AL, USA
mmcmeen@stiusa.com