Functional and SIR testing on the Same Assembly under Powered Conditions by Investigating Assembly Processes per IPC Std J-001H -Section 8: Cleanliness

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Abstract

Electronic device reliability is more challenging due to various factors related to increased functionality, component miniaturization and design, electrification, assembly process, and the demands of the user environment. Factors such as ambient humidity and temperature conditions, day/night temperature variations, cleanliness of the electronic circuitry, PCBA design, and surface characteristics all influence device reliability.

To properly assess the effects of process residues during manufacturing, the industry needs additional tools (beyond visible inspection and periodic ROSE testing) that measure active circuity change when exposed to environmental conditions. Assessing residues during the manufacturing with SIR (surface insulation resistance) compared to functional circuitry on the same assembly determines the interactive effects of two SMT reflows, selective wave solder, and rework/repair conditions on the test assembly. This allows understanding of IPC SIR limits to critical sensitive circuits, LED, battery, clock, high impedance, microprocessor high speed, and RF circuits.

A designed experiment using a data collection board to study the functional effects of circuitry in combination with surface insulation resistance will be performed. The objective is to evaluate the impact of component types, geometries, layout, flux type, and cleanliness methods on circuit reliability. The test instrument allows the user to look at the conditional effects of process residue to assess sensitivity while providing meaningful information on the causes of process failures and the root cause that drove these failures to occur. The research compares no clean and cleaned assembly processes under 40°C/90% RH.

Introduction

Flux and process residues from all process steps are collected on the active circuit traces, pad-to-pad, via-to-pad, and hole-to-hole spacing.[1] Component pitches have reduced while board density has increased. Electrochemical failures (parasitic leakage and/or dendrite formation) are point-specific.

As trace gaps and component geometries decrease, there is a need to validate electrical performance using electrical test methods. Testing the assembly under accelerated test conditions using high temperature, high humidity, and electrical bias enables the assembler and design authority to understand product reliability by speeding up possible faults. The electrical properties are evaluated during testing to determine product reliability under severe conditions. As the test voltage and pitch of the test pattern are reduced, surface insulation resistance (SIR) values drop.

Climatic conditions (temperature and humidity) directly impact an electronic device's functioning, lifetime, and overall reliability.[2] High humidity dissolves ionic contaminants by increasing leakage currents (metal oxide alignment) on the surface of printed circuit boards, which reduces surface insulation resistance. The threshold relative humidity for the SIR failures in the circuitry is greatly affected by the type and amount of ionic contamination present on the printed circuit board assemblies (PCBAs).[3]

Electronics manufacturers aim to minimize the amount of flux residues. Solder flux residues are a significant source of ionic contamination on the manufactured PCBAs, and the activator type in the flux determines their corrosiveness. The risk occurs on low standoff components, such as the QFN, due to blocked flux outgassing channels. The second risk is the number of soldering process steps used to build the assembly. Selective soldering, wave soldering, manual, and rework soldering can spread flux residues across the assembly. Pockets of active residue can be present when the flux is not fully heat-activated. For high reliability, the best practice is to clean the assembly.

SIR (Surface Insulation Resistance) Testing

SIR detects the effects of ionic residues that can cause intermittent and total failure. SIR testing uses an industry-standard pattern of traces (called a comb) to test the conductivity of process residues by combining environmental moisture, temperature, and bias voltage in a test chamber and monitoring electrical resistance over 7-days.

Testing is commonly performed over 168 hours at 40°C and 90% relative humidity and biased at 5 Volts DC. A test measurement of the insulation resistance is taken every 20 minutes. Insulation Resistance is charted in $Log_{10}\Omega$s on the Y-Axis. Time in hours was charted on the X-Axis. The chart below is divided into three zones:

1. Desirable Performance Range: Green Passing
2. Cautionary Performance Range: Yellow – Passing
3. Danger Zone: Red - Fail

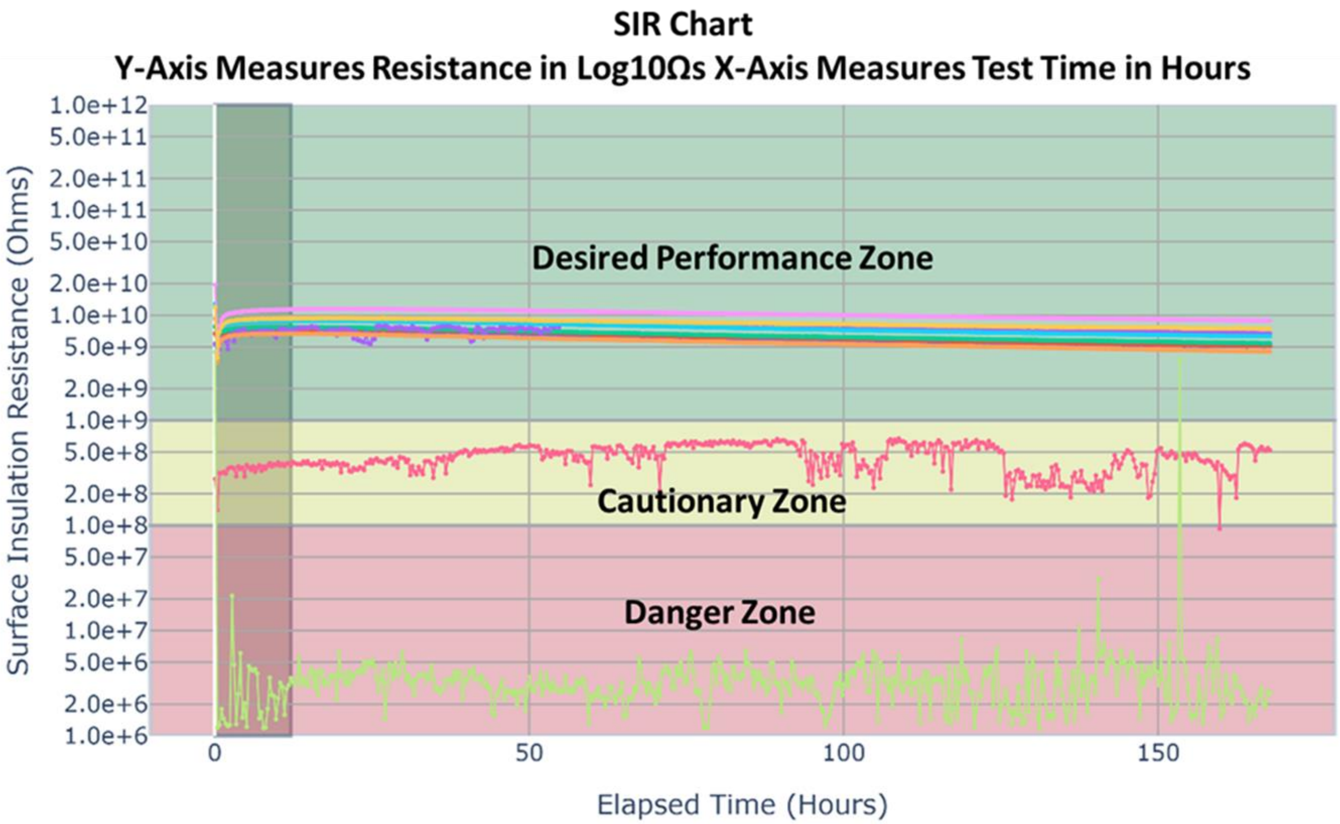


Figure 1: SIR Chart illustrating Danger, Cautionary, and Desired Performance Zones

At elevated humidity, adsorbed moisture creates a medium for ionic flux activators to dissolve into water. When ionic flux activators are present, they dissolve in water to form an electrolyte. The applied voltage initiates a REDOX (Oxidation/Reduction) reaction. The reactions produce ions that move through the liquid. The movement of the charged ion creates the current. The positively charged metal ions are attracted to the negative side of the circuit. When the metal ion reaches the negative side, it reduces (receives electrons) and plates as metal dendrites. These leakage currents drop insulation resistance, resulting in intermittent and total device failures.

Transient moisture on the device dissolves ionic contamination. When metal oxides are dissolved into the electrolyte, they will migrate from the positively charged anode and plate backward from the cathode to the anode, causing electrochemical migration in dendrites. Figure 2 illustrates the steps that lead to leakage currents and dendrite shorting.

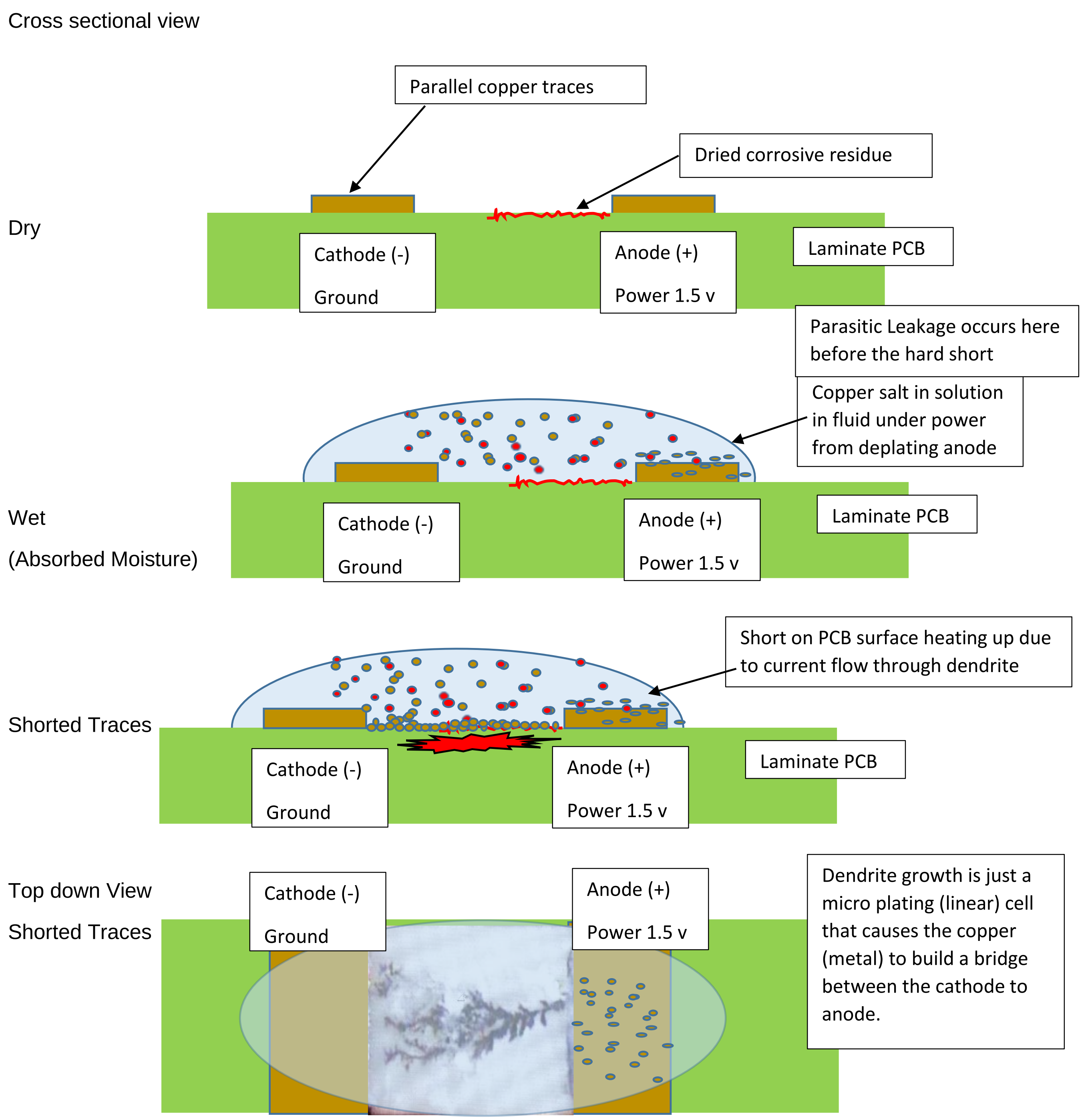


Figure 2: Conditions that Drive Leakage Currents and Dendritic Growth

Functional (FCT) Testing

Printed Circuit Boards are functionally tested to confirm PCBA performance. This testing process is the last leg of the assembly process before shipment. Functional (FCT) Testing objective is to evaluate the board's overall performance. The primary aim of this testing procedure is to discover some of the issues or lagging performance factors that could make the PCB unable to reach its full potential. The core issues commonly detected are voltage inaccuracy, power issues, and signal distortion. [4]

Passive components, including resistors, capacitors, inductors, and circuit-protection devices, comprise the highest percentage of all devices assembled on today's PCB assemblies. However, the successful isolation and testing of these components during ICT (in-circuit testing) is perhaps the most challenging and the least understood of all modern-day validation practices.[5]

In-circuit testing (ICT) identifies manufacturing process defects and component defects. ICT operates by gaining direct electrical access to the board under test through a bed-of-nails fixture and other limited-access techniques, including IEEE 1149.1 boundary scan and IEEE 1149.8.1 powered opens.[5] When performing electrical tests, each active and passive component is typically isolated from other surrounding components and tested individually. The limitation of ICT is the lack of temperature and humidity, which significantly influences leakage currents.[6]

The highly accelerated temperature and humidity stress test (HAST) tests the reliability of electronic components using temperature and humidity as environmental parameters.[7] The purpose is to evaluate a test sample's humidity resistance by increasing the water vapor pressure in a test chamber to an extremely high level above the partial water vapor pressure inside the sample. This process temporally accelerates the infiltration of moisture into the sample. When ionic contamination is present, moisture bonds with the ionic contaminant, which drives electrochemical failures.

Functional testing drives more toward the electrical performance of live components. Complex components, such as integrated circuit packaging, contaminate the component's interior from the manufacturing process or flux outgassing.[6] Does the process contamination cause drift or lagging performance on these functional circuits? In combination with the functional components, populating the test board with comb structures under components with no active circuitry enables SIR testing under component terminations. Exposing the test board to harsh environmental conditions within an environmental chamber at a specific temperature, humidity, and bias detects the effects of flux and process residue on the functional and non-functional (dummy) components. Testing functional and SIR circuits on the same test board improves the ability to detect the impact of process contamination and component defects on live (functional) and biased comb patterns under component terminations (SIR).

Research Hypothesis

The research hypothesis in this study expects a functional component performance change (lag - over biasing - under biasing) when surface insulation resistance drops due to the formation of leakage currents.

Functional / SIR Test Vehicle

The test board is designed with functional, CAF, and SIR test circuits monitored under power. The test assembly is a tool to understand the material effects under SIR conditions using different component structures. The test board is designed to test the interactive effects of the collective residues from multiple soldering steps, whether No-Clean or Cleaning, on functional circuits and their interactivity in typical operation conditions. This shows why a short in one area will cause a failure at a separate part of the circuit with just a few ohms of leakage on sensitive circuits that may or may not recover. SIR misses the effect of circuit sensitivity on functional performance, and this test vehicle is the first step to creating this understanding.

The front side of the test board design in Figure 3 contains the following components.

- SIR components
    - 8-pin SIR header
    - BGA, inner and out balls
    - 2 (0805) resistors to SIR pad
    - 6 CAF via pairs and plane test
- Functional components
    - Solder continuity BGA.
    - Coin cell battery.
    - RF Wireless circuit and antenna
    - Real-time clock
    - Temperature Monitor
    - Humidity Monitor
    - Switch/LED
    - Cap leakage current (whiskers)

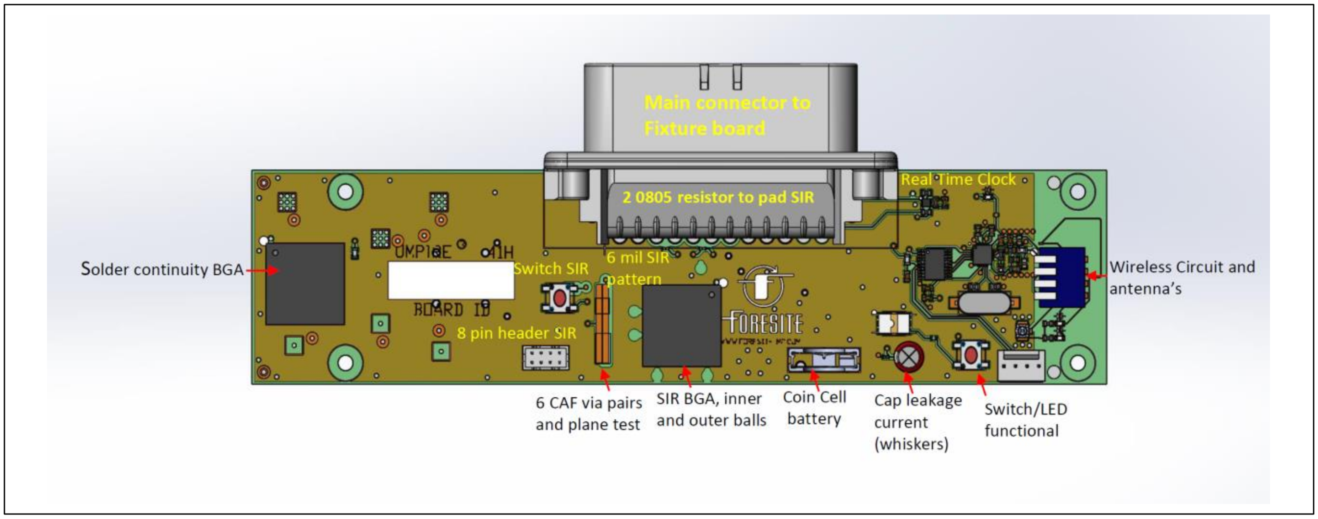


Figure 3: Front side of the Functional / SIR Test Board

The back side of the board design in Figure 4 contains the following components.

- SIR Components
  - 2 (0805) resistors to SIR pad
  - PQFP SIR over leads and Comb pattern under part
  - 3 raised QFNs
  - 3 standard QFNs
- Functional Component
  - High Impedance Circuit
  - Core Voltage Circuit Monitoring

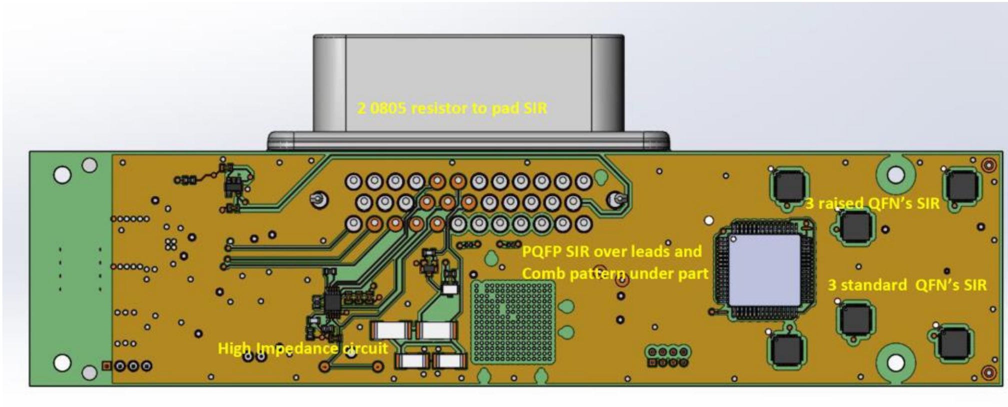


Figure 4: Back side of the Functional / SIR Test Board

Data Collection

The identifier/location assigned to each component during testing is a crucial reference point for determining the circuit board's X, Y, and Z (Front/Back) coordinates. These coordinates are used to precisely locate and display an image of the circuit board, facilitating visual inspection and analysis of individual components within the context of the entire board.

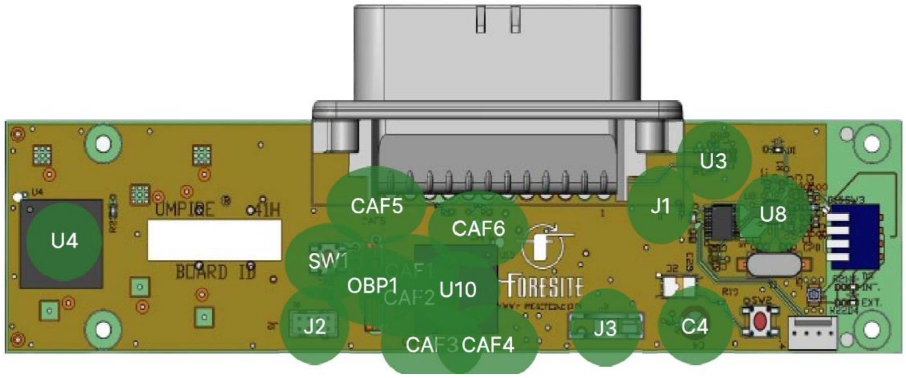


Figure 5: Components Locations on the Top Side of the Test Board

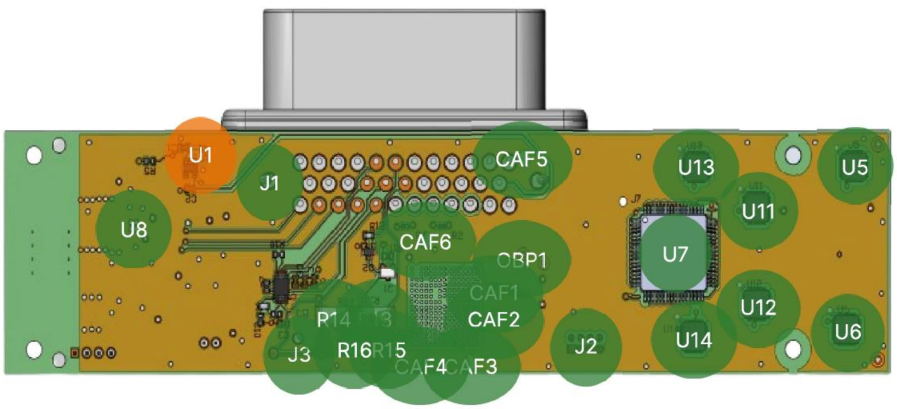


Figure 6: Component Locations on the Back Side of the Test Board

Criteria

1. Binary: Detects a simple pass/fail outcome. It’s typically used when there is a clear yes/no, on/off, or true/false condition to evaluate.
2. Range: Checks whether a numerical value falls within a specified range or interval. Once the minimum and maximum value is established, the status is determined based on whether the actual value falls within the range.
3. Maximum: A maximum allowable value for a numerical parameter is established. If the actual value exceeds this maximum, it triggers a specific status.
4. Minimum: A minimum required value for a numerical parameter is established. If the actual value is below this minimum, it results in a particular status.

Table 1: Numerical Outputs – Criteria Setup

Component	Location	Minimum	Maximum	Unit	Criteria	Warning
Battery Voltage	J3	1.3	3.6	V	Standard	5%
250µF Capacitor Leakage Current	C4	0	35	mA	Standard	5%
High Current	R13 – R16	200	230	mA	Standard	5%
3.3 V Rail	U1	3.135	3.465	V	Standard	5%
Temperature				°C	Custom	5%
Humidity				%	Custom	5%
Main Connector SIR	J1	100 megΩ		Ω	Standard	5%
BGA Outer SIR	U10	100 megΩ		Ω	Standard	5%
BGA Inner SIR	U10	100 megΩ		Ω	Standard	5%
Switch SIR	SW1	100 megΩ		Ω	Standard	5%

Comb SIR	U7	100 megΩ		Ω	Standard	5%
8-pin connector SIR	J2	100 megΩ		Ω	Standard	5%
Probe SIR	OBP1	100 megΩ		Ω	Standard	5%
QFN1 SIR	U5, U11, U12	100 megΩ		Ω	Standard	5%
QFN2 SIR	U6, U13, U14	100 megΩ		Ω	Standard	5%
PQFP SIR	U72	100 megΩ		Ω	Standard	5%
CAF Via Resistance	CAF1	100 megΩ		Ω	Standard	5%
BGA Solder Joint			500	Ω	Standard	5%

Clarifications:

- Standard is a criterion that is defined.
- Custom is criteria set per test or defined by the user.
- The user defines a warning trigger.
- Binary criteria are non-customizable and rely on the straightforward assessment of whether a signal is received.

Experimental Methodology

Four Test Boards were assembled with a ROL0 Low Residue No-Clean SAC 305 Solder Paste. The test boards were ***not*** cleaned after assembly. The test boards were hooked up to the Functional / SIR Test instrument. The test boards were placed into an environmental chamber at 40°C / 90% Relative Humidity / 5 Volts Bias / 10-minute measurement cycle. The temperature and humidity were charted from sensors placed on the test boards.

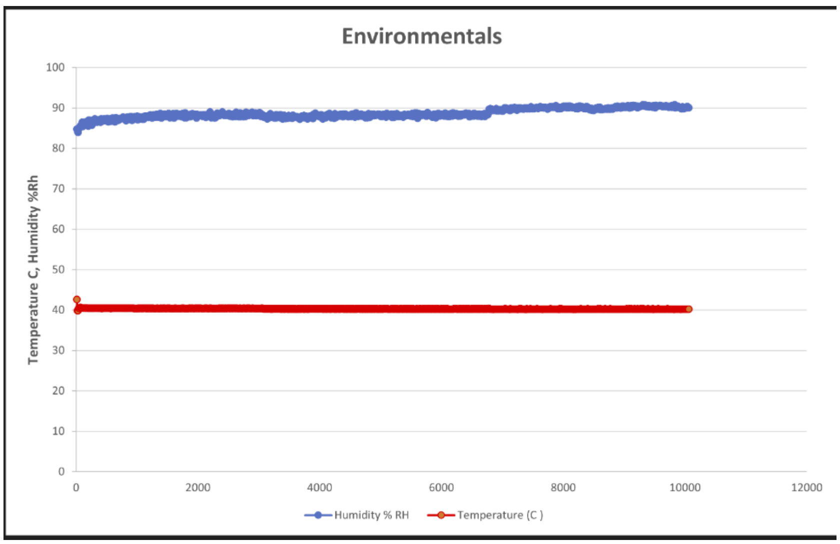


Figure 7: Environmental Conditions over the Testing Period

Results

The test results provide insights into the status of the Functional and SIR Circuits. The outputs for Coupon 1 illustrate areas of the test board where components function correctly and where failures occur. Figure 8 provides the results for the Top Side of one of the test boards.

Top Side of the Test Board

Sensors	Location	Criteria	Actual	Status
Wireless Module	U8	Binary	1 - 1	PASS
Battery Voltage	J3	1.3 - 3.6 (±5%)	3.116 - 3.283	PASS
250uF Capacitor Leakage Current	C4	Max: 35 (±5%)	0.008 - 0.12	PASS
Temperature	U3	-100 - 300 (±5%)	103.739 - 108.685	PASS
Humidity	U3	Max: 100 (±5%)	83.959 - 90.789	PASS
Main Connector SIR	J1	Min: 100 (±5%)	80 - 65535	FAIL
BGA Outer SIR	U10	Min: 100 (±5%)	80 - 637	FAIL
BGA Inner SIR	U10	Min: 100 (±5%)	60539 - 65535	PASS
Switch SIR	SW1	Min: 100 (±5%)	65535 - 65535	PASS
8 Pin Connector SIR	J2	Min: 100 (±5%)	576 - 2101	PASS
Probe SIR	OBP1	Min: 100 (±5%)	65535 - 65535	PASS
CAF VIA Resistance	CAF1, CAF2, CAF3, CAF4, CAF5, CAF6	Min: 100 (±5%)	65535 - 65535	PASS
BGA Solder Joint	U4	Max: 500 (±5%)	0 - 0.734	PASS

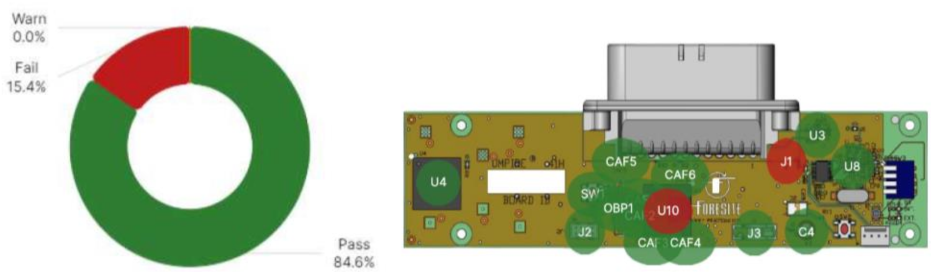


Figure 8: Test Results for the Top Side of the Board

The J1 main connector failed SIR testing. This indicates the selective solder flux left active (ionic) flux residue across the thru-hole connections.

- Board 1 left an active residue with a leakage current detected early in the test period, which dropped below 8 Log $^{10}\Omega$s. SIR slowly improved over the testing period while still showing signs of activity.
- Board 2 was stable and in the desired performance zone but formed a leakage current that dropped insulation resistance by roughly two decades.
- Boards 3 and 4 were stable and in the desired performance zones.

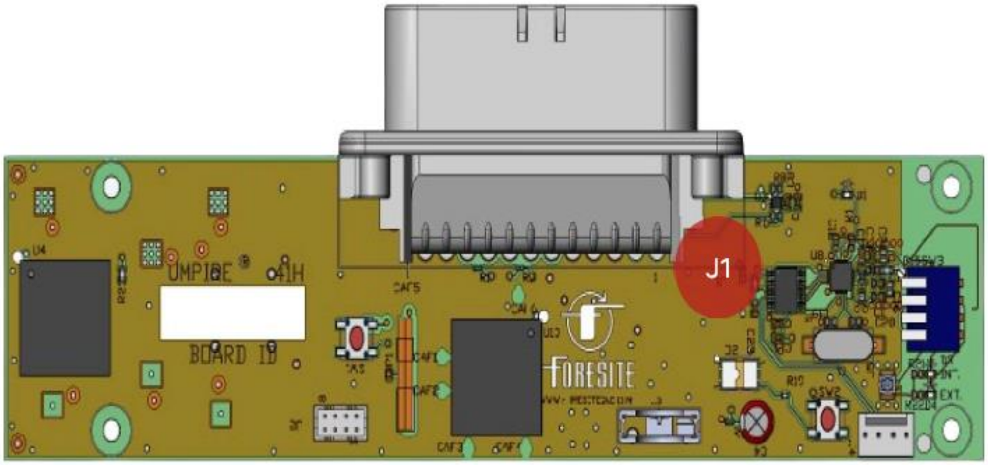
Coupon **1**

Main Connector SIR FAIL

Sensor Code: H000 | **Type:** MainIOConnector | **Technology:** PTH

Location

Board Location	J1
Board Side	Top / Bottom
Connector Pins	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35



Insights

Criteria	Min: 100 (±5%)
First Failure	10/25/2023, 5:02:52 PM
Standard Deviation	5254.27
Max	65535
Min	80
Average	2029.941351888668

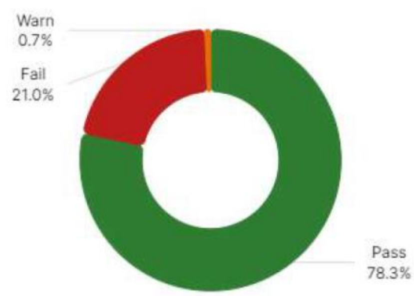


Figure 9: J1 Connector Front Side

Figure 9: J1 Failure

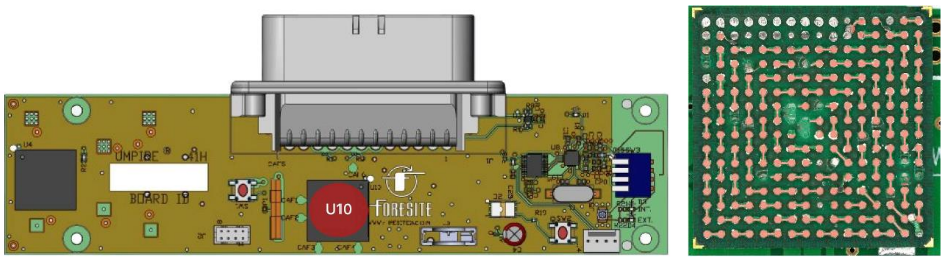
- BGA Outer SIR (U10)
    - Board 1 started in the failure zone while slowly improving to the cautionary zone.
    - The failure was due to flux residues that were not fully outgassed.
    - Boards 2, 3, & 4 were stable and in the desired performance zones.

Coupon **1**

BGA Outer SIR FAIL

Sensor Code: H001 | **Type:** BGADaisyChain | **Technology:** SMT

Location	
Board Location	U10
Board Side	Top
Connector Pins	19



Measurements

Insights	
Criteria	Min: 100 (±5%)
First Failure	10/25/2023, 12:12:52 PM
Standard Deviation	143.93
Max	637
Min	80
Average	324.85188866799206

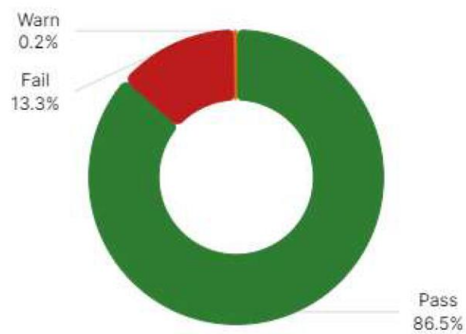


Figure 10: BGA Outer Front Side of the Board

Bottom Side of the Test Board

The bottom side of the test board found issues with 3.3 Volt Rail, J1 main connector, and QFNs.

Sensors	Location	Criteria	Actual	Status
Wireless Module	U8	Binary	1 - 1	PASS
Battery Voltage	J3	1.3 - 3.6 (±5%)	3.116 - 3.283	PASS
High Current	R13, R14, R15, R16	200 - 230 (±5%)	215.835 - 216.129	PASS
Test Coupon 3.3.v Rail	U1	3.135 - 3.465 (±5%)	3.322 - 3.322	WARN
Main Connector SIR	J1	Min: 100 (±5%)	80 - 65535	FAIL
Comb SIR	U7	Min: 100 (±5%)	65535 - 65535	PASS
8 Pin Connector SIR	J2	Min: 100 (±5%)	576 - 2101	PASS
Probe SIR	OBP1	Min: 100 (±5%)	65535 - 65535	PASS
QFN1 SIR	U5, U11, U13	Min: 100 (±5%)	80 - 65535	FAIL
QFN2 SIR	U6, U12, U14	Min: 100 (±5%)	21620 - 65535	PASS
PQFP SIR	U7	Min: 100 (±5%)	80 - 65535	FAIL
CAF VIA Resistance	CAF1, CAF2, CAF3, CAF4, CAF5, CAF6	Min: 100 (±5%)	65535 - 65535	PASS

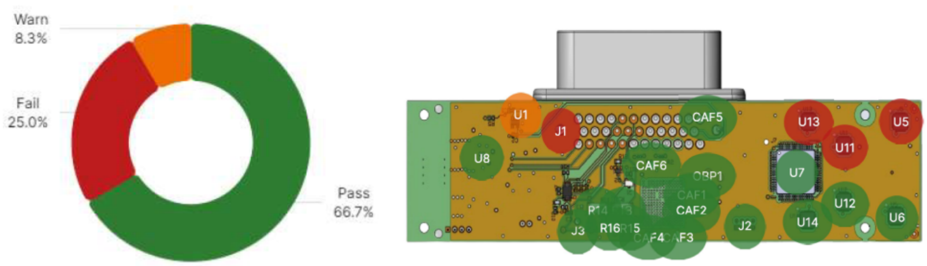


Figure 11: Test Results on the Back Side

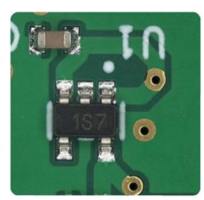
- 3.3 Volt Rail (U1) found parasitics leading to a cautionary condition.

Coupon 1

Test Coupon 3.3.v Rail WARN

Sensor Code: E000 | **Type:** FunctionalPowerCircuit | **Technology:** SMT

Location	
Board Location	U1
Board Side	Bottom
Connector Pins	23



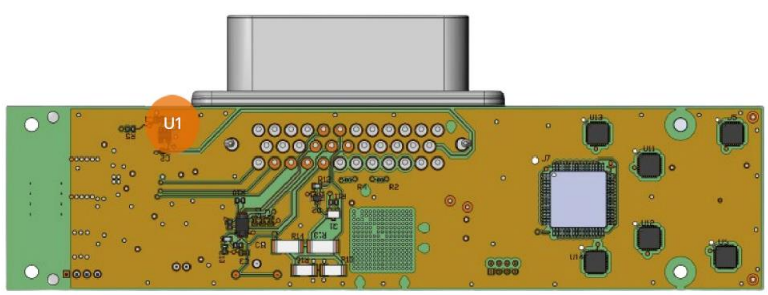


Figure 12: 3.3 Volt Rail

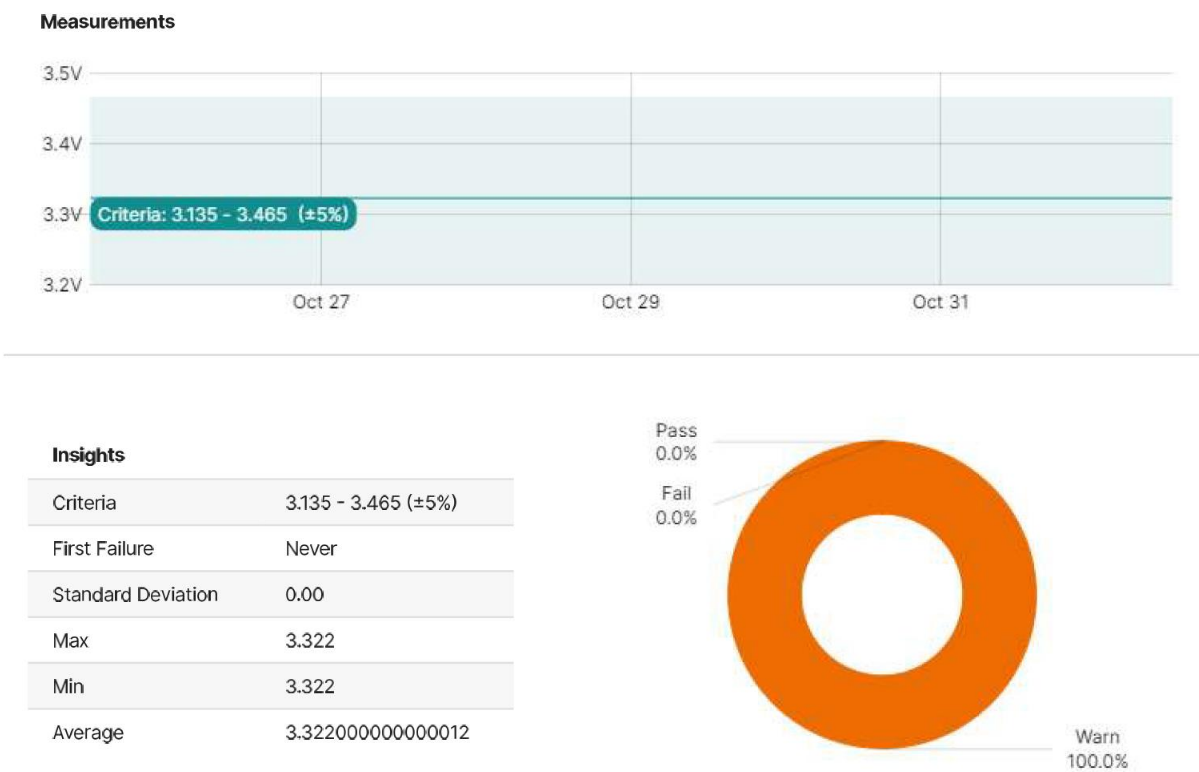


Figure 13: 3.3 V Rail Stats

The J1 main connector failed SIR testing. This indicates the selective solder flux left active (ionic) flux residue across the thru-hole connections.

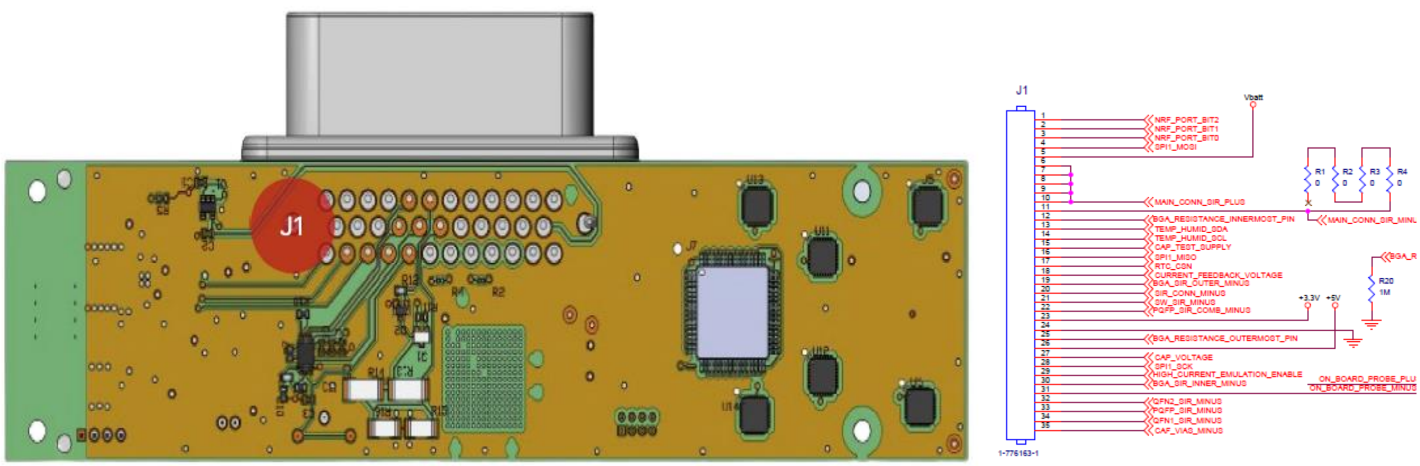


Figure 14: J1 Connector on the Back Side of the Test Board

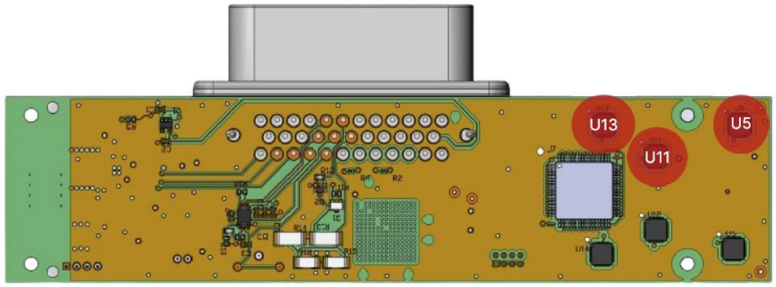
Two sets of QFNs were placed on the back side of the test board. U5, U11, and U13 had standoff gaps of 25-50µms. These QFNs failed. Conversely, QFNs U6, U12, and U14 were raised using preforms to a gap of 100-150µms. These QFNs passed—low standoff gaps block flux outgassing. The negative result is higher volumes of flux residues and pockets of active flux.

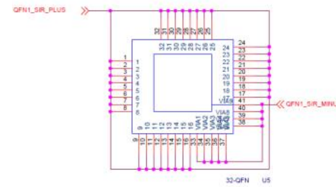
Coupon **1**

QFN1 SIR **FAIL**

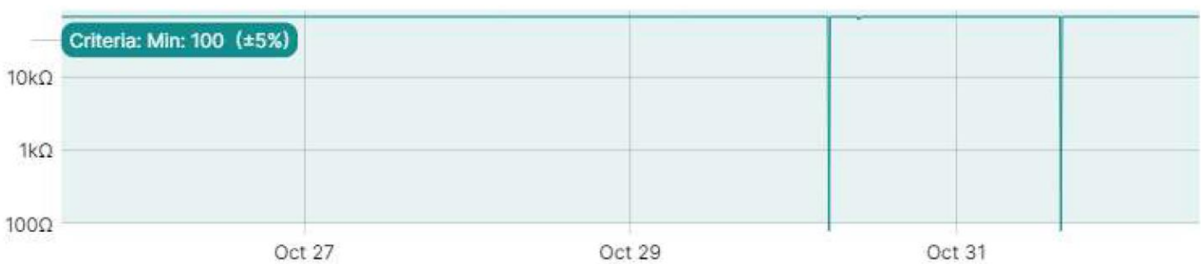
Sensor Code: H007 | **Type:** PQFNSIR | **Technology:** SMT

Location	
Board Location	U5, U11, U13
Board Side	Bottom
Connector Pins	34





Measurements



Insights	
Criteria	Min: 100 (±5%)
First Failure	10/30/2023, 5:12:52 AM
Standard Deviation	2923.66
Max	65535
Min	80
Average	65394.92047713718

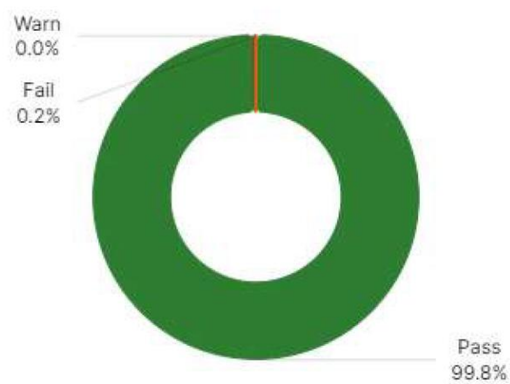


Figure 15: QFNs with Standard Standoff Gaps

- PQFP (U72) SIR has a comb structure under the component termination. The comb structure is sensitive to selective solder flux that wets neighboring components and to wash fluids that are not adequately rinsed. This failure was likely due to selective solder flux wetting to the QFP component. When this occurs, the no-clean flux has not been fully heat-activated, leaving behind an ionic residue susceptible to failures when exposed to harsh conditions.

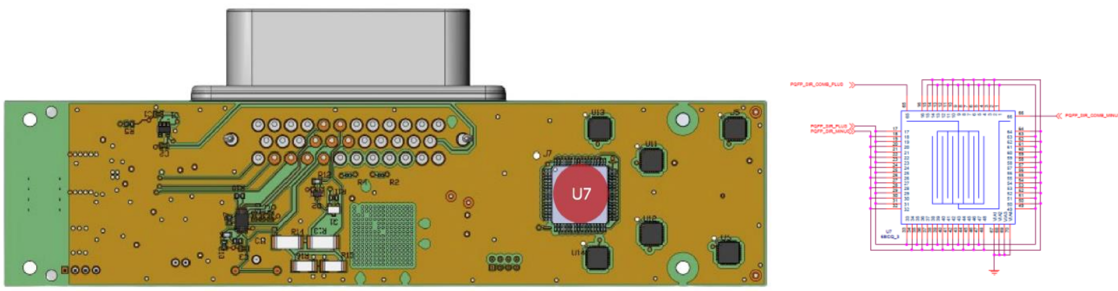
Coupon
1

PQFP SIR FAIL

Sensor Code: H009 | **Type:** N/A | **Technology:** SMT

Location

Board Location	U7
Board Side	Bottom
Connector Pins	33



Measurements

Insights

Criteria	Min: 100 (±5%)
First Failure	10/27/2023, 2:12:52 AM
Standard Deviation	4119.16
Max	65535
Min	80
Average	65274.74155069583

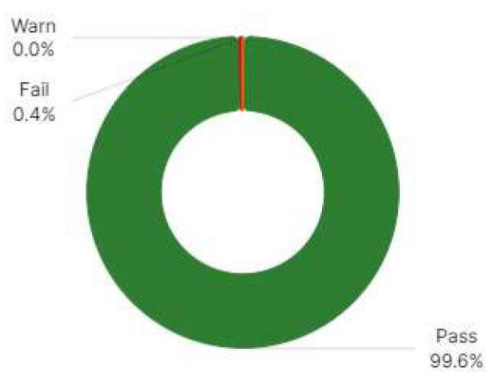


Figure 16: PQFP with a SIR Comb under the Component Termination

Inferences from the Data Findings

SIR is an electrical test method performed on test boards representative of the process conditions.[8]

1. Electrical resistance of an insulating material between contacts, conductors, or grounding devices.
2. The test is run under specified environmental and electrical conditions.
3. SIR tests for the effects of PCBA manufacturing and electronic assembly process residues and their impact on reliability.
4. The test boards are exposed to high humidity and temperature [i.e., 40°C/90% RH].
5. Used to evaluate a product's ability to resist "failure" due to current leakage or electrical shorting (i.e., dendritic growth).

Four components failed SIR testing. The data provides insight into the components most susceptible to trapping active residues.

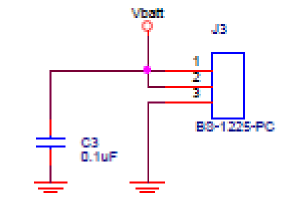
Sensors	Location	Criteria	Actual	Status
Main Connector SIR	J1	Min: 100 (±5%)	80 - 65535	FAIL
BGA Outer SIR	U10	Min: 100 (±5%)	80 - 637	FAIL
BGA Inner SIR	U10	Min: 100 (±5%)	60539 - 65535	PASS
Switch SIR	SW1	Min: 100 (±5%)	65535 - 65535	PASS
Comb SIR	U7	Min: 100 (±5%)	65535 - 65535	PASS
8 Pin Connector SIR	J2	Min: 100 (±5%)	576 - 2101	PASS
Probe SIR	OBP1	Min: 100 (±5%)	65535 - 65535	PASS
QFN1 SIR	U5, U11, U13	Min: 100 (±5%)	80 - 65535	FAIL
QFN2 SIR	U6, U12, U14	Min: 100 (±5%)	21620 - 65535	PASS
PQFP SIR	U7	Min: 100 (±5%)	80 - 65535	FAIL
CAF VIA Resistance	CAF1, CAF2, CAF3, CAF4, CAF5, CAF6	Min: 100 (±5%)	65535 - 65535	PASS
BGA Solder Joint	U4	Max: 500 (±5%)	0 - 0.734	PASS

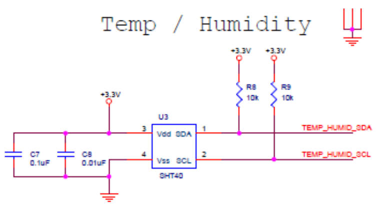
Figure 17: SIR Data Findings for Each Component on the Test Board

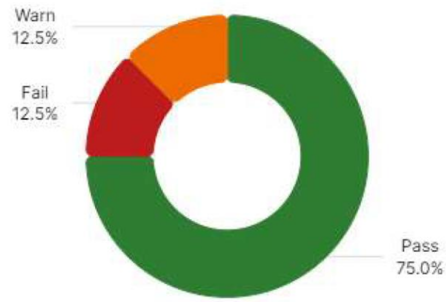
The functional components that exhibited issues were the real-time clock and 3.3-volt rail.

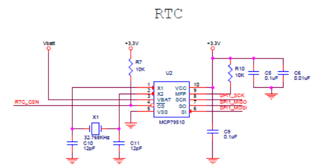
Coupon 1

Functional Overview FAIL









Sensors	Location	Criteria	Actual	Status
Wireless Module	U8	Binary	1 - 1	PASS
Battery Voltage	J3	1.3 - 3.6 (±5%)	3.116 - 3.283	PASS
250uF Capacitor Leakage Current	C4	Max: 35 (±5%)	0.008 - 0.12	PASS
High Current	R13, R14, R15, R16	200 - 230 (±5%)	215.835 - 216.129	PASS
Test Coupon 3.3.v Rail	U1	3.135 - 3.465 (±5%)	3.322 - 3.322	WARN
Temperature	U3	-100 - 300 (±5%)	103.739 - 108.685	PASS
Humidity	U3	Max: 100 (±5%)	83.959 - 90.789	PASS
Realtime Clock		Binary	NaN - NaN	FAIL

Figure 18: Functional Components on the Test Board

Discussion

Cleanliness of materials, components, and manufacturing processes are integrated as the overall PCBA contamination level and extent are determined by the contribution from the components, standoff gap, and reflow soldering process. This directly connects to the use of “no-clean” flux since removing flux residue during the soldering process depends on the kinetics of the thermal decomposition process, which is never complete due to variations in the temperature profile and short exposure time to higher temperatures.[9]

Industries face more issues today due to the change in manufacturing processes. Multiple assembly processes make the task of mapping and specifying the residues more difficult. Miniaturization of electronics means smaller PCB layouts, smaller components, lower standoffs, and multiple PCB layers. The process is seldom clean for assemblers who build “No-Clean” assemblies, leaving significant residues under component terminations. For assemblers who “Clean,” the difficulty of removing residues under component terminations can leave behind partially cleaned flux residues.

A test instrument designed to test functional, CAF, and SIR test circuits monitored under power enables the assembler and design authority to validate the process conditions used to build the assembly. Performing the test with environmental conditions that expose the assembly to temperature, humidity, and bias factors in the effects of process residues during functional testing. The idea is a “Process Validation Tool” that tests the design's robustness in settings consistent with the end-use environment.

The research test boards were assembled with a high-reliability No-Clean Solder Paste. The data findings illustrate latent defect issues on functional components and leakage currents detected on the SIR circuits below.

1. We see acceptable but noisy results from the wave solder process in the SIR of the main connectors J1 and J2. When we look at the battery circuit and the cap circuit, we see a consistent drop in the voltage due to leakage paths from the wave flux but no issues on the bottom or top of the resistor. This indicates that the flux spread was minimal, but the entrapment impacted performance.
2. The SIR of the PLCC and QFN show acceptable noisy levels, but the performance of the high impedance R13 -R16, voltage Rail U3, and thermal measurement indicate SMT residues causing leakage performance issues.
3. It is crucial to understand the SIR conditions. Still, we must learn at what points we impact circuit performance based on SMT, wave, or the interaction between the assembly processes and fabrication effects.
4. Whether the process is "No-Clean" or "Cleaned Assemblies," the reflow soldering process significantly contributes to overall reliability. SIR detects the effects of process residues and their impact on functional performance.

Conclusions

Combining functional and SIR testing enables the design authority to detect parasitic residue effects on sensitive parts of critical circuits while detecting the impact of process residues on SIR circuits. Understanding the material effects under SIR conditions and the interactive effects of the collective of residues from the multiple soldering/cleaning, or soldering and No-Clean operations, on the functional circuits and their interactivity in typical operation conditions provides process data to enable a reliable design. The goal is to show the effect of why a short in one area will crash a separate part of the circuit with just a few ohms of leakage or sensitive circuits that may or may not recover. SIR misses the effect of circuit sensitivity on functional performance. The test instrumentation and test vehicle design are the first steps to creating this understanding.

Acknowledgments
The authors want to acknowledge the engineering and software teams who worked to develop and prove the test instrument.

- Jim Gryga, Lead Electrical Engineer
- Steve Middleton, Electrical Engineer
- Paco Solis, Lead Investigator
- Bobby Glidwell, System Architect
- Anna Ailsworth, User Experience Lead
- Kyle McCarty, Backend Developer
- Zach Papiez, Chemical Engineer
- Adam Klett, Ph.D., Director of Science

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