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REAL-TIME RELIABILITY TESTING ADVANCEMENTS ON PRODUCTION ELECTRONIC HARDWARE

ABSTRACT

OEMs (Original Equipment Manufacturers) and EMSs (Electronic Manufacturing Services) work to a set of guidelines and test procedures for qualification of hardware when changing soldering materials, process conditions, cleaning materials, cleaning machines, and conformal coating. Evaluation and use of any soldering material, reflow setting, or cleaning material, the EMS *shall* confirm that the proposed materials are characterized and qualified to the applicable ANSI/IPC Industry Standards. Additionally, IPCJ-STD-001G, Amendment 1 issued changes to Cleanliness Standards requiring the assembler to develop objective evidence that a specific cleanliness condition renders a reliable device.

For many PCB designs with complex component geometries, cleanliness can impact reliability and circuit performance. The gold standard for circuit qualification has been to pass SIR (Surface Insulation Resistance) testing with resistivity values that show that the design and process do not interfere with the circuit performance. Up until now, SIR testing hasn't been practical on the manufacturing floor as the test traditionally takes seven days to complete, and requires equipment that is complicated to use. The purpose of this research is to design instrumentation and test methods that allow both the OEM and EMS to perform process development and process control using electrical test methods for use in an operations environment.

The research study centers on “*On-going Reliability Testing*” that allows the assembler to take testing to the technician level. Using a combination of modern, configurable test cards that scrutinize high-risk circuits and devices integrated on the assembly, the EMS can correlate cleanliness to production hardware. This bottom-up testing methodology allows the assembler to repeat IPC testing in their factory – objective evidence to J-STD-001G, Amendment 1. Also, they can expand testing to other areas such as system design, process development, process control, and quality assurance.

Keywords: Bottom Terminated Components, Electrochemical Migration, Dendritic Growth, J-STD-001, Flux Residues, Reliability, Warranty, Surface Insulation Resistance

CLASS 3 ELECTRONICS

The electronics industry has seen rapid growth over the past 50 years, with performance and cost declines beyond what

anyone could image⁸. Reliability and Safety of electronic hardware are of high importance to Class 3 industries such as Defense, Aerospace, Medical, and Automotive. The complexity of electrical systems can affect long-term reliability, leading to premature failure of the systems that employ them.

Aerospace and Defense Electronics:

Today's aerospace, space-based systems, and defense industries depend on electronics and PCBs¹². However, the quality requirements and reliability for aerospace & defense electronics are far more stringent than those for commercial electronics products. Aerospace and defense industry suppliers must adhere to specific standards and regulations meant to ensure the quality, reliability, and security of PCBs and their components. To meet this high bar, electronics developers need to employ process control measures to ensure that products, as well as processes, are reliable and work on demand.

Automotive Electronics

The automobile of the future will become an “Intelligent Vehicle¹³.” The human-machine interface requires Intelligent Sensors combined with Intelligent Actuators with the driver input through navigation, coordination, and monitoring. Intelligent sensors coordinate telematic information, position, kinetics, environment, and internal data. Intelligent actuators monitor the airbag system, brakes, steering, engine, transmission, electromechanical systems, and thermo-mechanical system.

Automotive electronics require consideration beyond conventional means to optimize board and component reliability¹⁴. The autonomous vehicle offers great potential for improvements in vehicular traffic, an increase in highway capacity and traffic flow, faster response times, less fuel consumption and less pollution. Designing in reliability is critical to ensure that vehicles operate safely in both daily traffic and harsh off-road environments.

Board level and microprocessor reliability rise in complexity due to the small scale of automotive electronics¹⁴. Temperature variations in combination with harsh environmental conditions can cause unwanted events and potential failures. Designing electronics systems to be robust against performance lags and degradation is critical to meet reliability expectations.

Medical Electronics

Medical devices – defined as any equipment used to diagnose, treat, or monitor patient health are subject to a variety of complex quality and safety analyses due to the potentially significant impact on human lives⁹. Numerous standards throughout the medical device industry require the use of a documented process to identify, analyze, and eliminate or control the risks associated with medical device hardware, software, and electronics. Risk management is the process of addressing potential risks throughout the entire product lifecycle of medical device products, including development, manufacture, maintenance, and disposal or decommissions.

Assessing and reducing the risks associated with medical devices helps to reduce the total impact of wide-ranging product recalls, including financial costs as well as reduced customer satisfaction and a damaged company reputation. Most importantly, companies are morally and ethically obligated to know the impact that a product will have on human safety and wellbeing before the product is released to the public.

CHEMICAL RESIDUES DECREASE RELIABILITY

Class 3 specifications and standards, which govern the development of high-tech systems have not kept pace with miniaturization and microelectronic component technology⁷. The performance and cost advances over the past 20 years have enabled technologies to advance beyond what anyone could have imagined⁸. In spite of these technology advances, the cleanliness standards that contractors rely on to ensure the design, production, and quality of next-generation Class 3 electronic hardware has remained unchanged. As technologies advance, the companies who build the device need guidance on what to do and how to do it⁷.

Electronic assemblies are prone to intermittent and total failure from process contamination¹¹. Contamination trapped under leadless components is highly problematic due to the pitch reduction, flux residues left under the body of leadless and bottom terminated components (Figure 1). Also, shadowing effects of high components next to bottom terminated components can leave active flux residue, which when exposed to harsh conditions can result in intermittent or device failure.

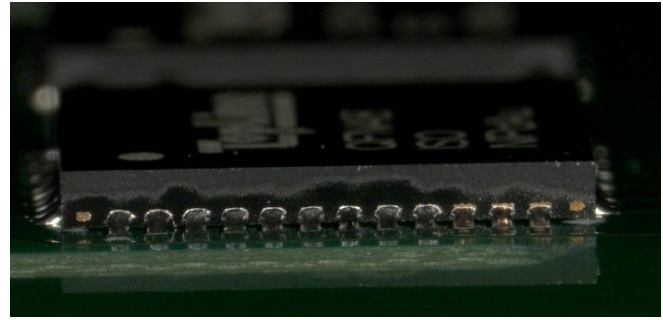


Figure 1: Flux Residues after Reflow on a BTC

Flux residues trapped under low standoff leadless components may still be active due to blocked outgassing channels, even when using a no-clean solder paste. Quantifying the risk of site-specific residues under problematic components is commonly done during the materials and process validation using chemical and electrical test methods. Process verification and validation are done to characterize and prove out the process on the materials used to build production hardware. Once the printed circuit assembly is placed into production, process control test methods to assure conformance are lacking.



Figure 2: Active Flux Residue under the BTC

This research is a call to change the way we think about reliability assurance regarding the cleanliness of Class 3 hardware. This approach suggests the following:

1. Materials and process characterization using both electrical and chemical test methods called out in the standards should not change.
2. Adopt improved process control methods for low-volume, high-reliability manufacturing.
3. Accept ownership for quality and reliability of all of the components and materials.
4. Quality and reliability of components, materials, and process parameters are the responsibility of those who manufacture them.

RISK MANAGEMENT

In the design and development of safe, effect devices, reducing risk and ensuring reliability are a manufacturer's first responsibility⁹. The advanced technology inherent in Class 3 hardware and their production means that all aspects of the system – including mechanics, electronics, software, and hardware must be evaluated for reliability. Every aspect of its development – from design and prototyping through manufacture, distribution, disposal, and decommissioning must adhere to strict quality standards that are documented and traceable to functional and safety requirements.

When risks are discovered, they must be evaluated for their severity and probability of occurrence, and eliminated or mitigated as appropriate. Continued performance and performance on demand requires the following considerations.

- **Part failures:** The failure of one part or component on an electrical device can lead to system failure and may result in human injury or death.
- **Human impact:** The potential harms caused by an electronic device failure may extend not only to the person but to others in the environment.
- **Advanced technology:** ICs have vulnerabilities that can affect long-term reliability, leading to premature failure of the systems that employ them⁸. These vulnerabilities are especially critical to Class 3 segments.
- **Product lifecycle:** Every aspect of the product development lifecycle for Class 3 electronic devices – form design, prototyping, assembly, decommissioning, and disposal must adhere to strict quality standards that are documented and traceable.
- **Industry standards:** These standards must apply to device manufacturers, suppliers, contractors, OEMs, third-party manufacturers, and others associated with product development and distribution. If device parts are manufactured by one company, assembled by another, and distributed by a third, all three parties should participate in the risk management process to ensure that every possible risk is managed before the device is sent to market.
- **Significant stakeholders:** A wide range of potential stakeholders are affected by the reliability of electronic devices, including government, industry, workers, family, and others. Risk mitigation is the responsibility of those associated with product development and distribution.

Risk management involves the systematic application of policies, procedures, and practices to the task of analyzing, evaluating, controlling, and monitoring the risk inherent in Class 3 hardware. Risk management is an iterative process that should assess all aspects of the product's lifecycle and must be implemented and documented throughout the design, development, prototyping, manufacture, and phases of a product's lifecycle to ensure that no new or unexpectedly severe risks go unmanaged.

RELIABILITY AS A FUNCTION OF CLEANLINESS

Northrup and Russeau (2018) stated: "The electronics industry has a growing need to understand the impacts of chemical residues on printed board (PB) and printed board assembly (PBA) reliability. Residues left from flux and other process chemistries can potentially lead to premature failure of assemblies once in the field. Understanding where such residues originate, and their impact on reliability is paramount to mitigating product failures due to cleanliness issues."

As components reduced in size, electrical clearance between conductors creates a reliability concern when flux residues are present. Since the area under these components is tiny, chemical extraction is no longer a reliable method for determining cleanliness levels. SIR is a reliable method for determining cleanliness levels under the body of components.

Surface Insulation Resistance (SIR) is the best method for testing electrochemical reactions at or below the surface of electronic circuits. Problematic residues will affect surface insulation resistance values. SIR testing is considered the gold standard and has been used for reliability testing since the development of the transistor. SIR is a highly sensitive instrument that is commonly offered by reliability labs. The test is expensive to run. Another limitation with using SIR is the length of time required to run a test and time required to crunch the data once the test is completed.

As a result of these limitations, most companies only use SIR when they are validating soldering and cleaning processes. Once the process is validated, process control is performed using chemical extraction methods. One of those methods is ROSE testing. Ion Chromatography is the preferred method, but it also is commonly performed by reliability testing labs. A site-specific method called "C3 extraction" is designed to extract at a component site or specific area on board. The C3 method is the closest method, but it too has limitations.

There is a need for a method that can be used at the production floor. Both the soldering and cleaning processes can drift over time. Residues are present under leadless and

bottom terminated components. These residues are not easy to detect and inspect. Cleaning under these components are also challenging. This risk to Class 3 contractors is a Cleanliness condition that can cause a reliability concern.

The defense industry issued a grant to study this issue. The research found that electrochemical testing by using SIR was the most effective method at detecting ionic residues on the surface and under component terminations. The project direction led to a focus on simplifying and developing a user-friendly instrument that enabled SIR testing at the production site. Key performance metrics included low-cost instrumentation, and test boards focused on problematic components, low-cost test boards, and software that processes the data real-time during the test. Processing the data real-time opens the window for using SIR for process control. If there is problematic residue present, SIR resistance levels drop within hours. The data provides a signal that an assembler can use to control their process.



Figure 3: SIR Instrumentation

The card view shows a red (failed), yellow (risk zone), and green (pass) after each reading during the test.

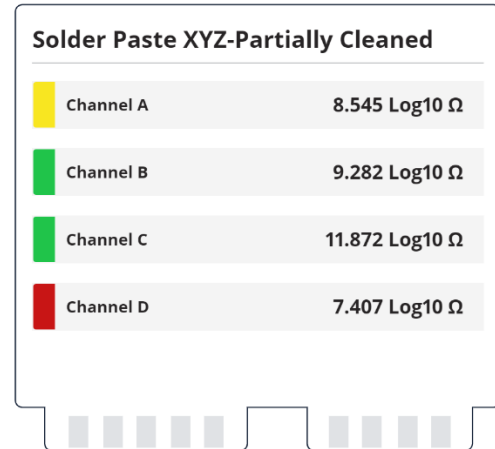


Figure 4: Card View

ON-GOING RELIABILITY TESTING

The risk management plan is designed to understand the impacts of chemical residues on printed board assemblies. The method includes criteria for risk acceptability based on industry standards. The standards provide the basis for accepting a particular risk when the probability of its occurrence or its potential harm cannot be eliminated, or rejecting the risk as being too hazardous and therefore requiring its elimination or mitigation.

Once a process is verified and validated, the cleanliness risk mitigation ensures that Class 3 manufactures electronics are reliable.

Step 1: Establishing acceptable and unacceptable levels of chemical residues on production hardware

Step 2: Identifying and analyzing the risks associated with contamination left on the device from all potential sources

Step 3: Implement control measures to eliminate risks or mitigate their effects

Step 4: Monitor the effectiveness of these controls

EXPERIMENTAL

A Class 3 Defense contractor requested a cleaning trial on a newly developed aqueous cleaning agent. The contractor provided three Solder Paste materials. They clean their assemblies in an inline aqueous cleaning tool.

Step 1: Establishing acceptable and unacceptable levels of chemical residues on production hardware

Factors investigated:

- Alternative cleaning material
 - Concentration: 15%
 - Upper Wash Pressure: 80 psi
 - Lower Wash Pressure: 60 psi
 - Upper Rinse Pressure: 60 psi
 - Lower Rinse Pressure: 40 psi
- No Clean Solder Paste

- SnPb Solder Paste #1
- SnPb Solder Paste #2
- Pb-Free Solder Paste #3
- Cleanliness
 - Not cleaned
 - Belt speed: 1 FPM
 - Belt speed: 2 FPM
- B-52 Legacy 3 Test Board (Figure 3)
 - QFN 48T, 0.5 Pitch
 - FBGA 244, 1 mm Pitch
 - QFP 80, 0.65 mm Pitch
 - QFP 160, 0.65 mm Pitch

Test Board

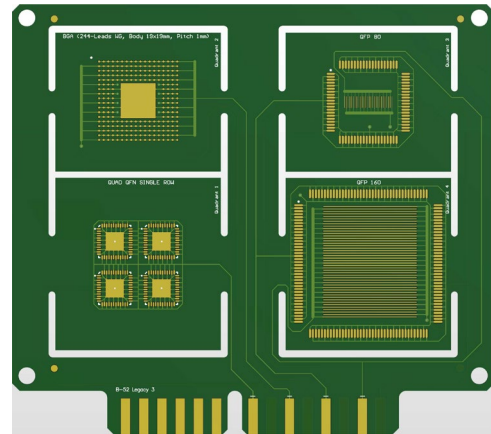


Figure 5: B-52 Legacy 3 Test Card

Data Findings

- Response
 - SIR (IPC-TM-2.6.3.7)
 - Voltage Bias: 8 volts
 - Temperature: 40°C
 - Relative Humidity: 90%
 - Time: 168 Hours

SIR values above 8 logΩ are considered to be in the desired performance zone¹⁶. SIR values in the range of 7 logΩ to 8 logΩ is deemed to be in the cautionary zone. SIR values below 7 logΩ are considered a failure.

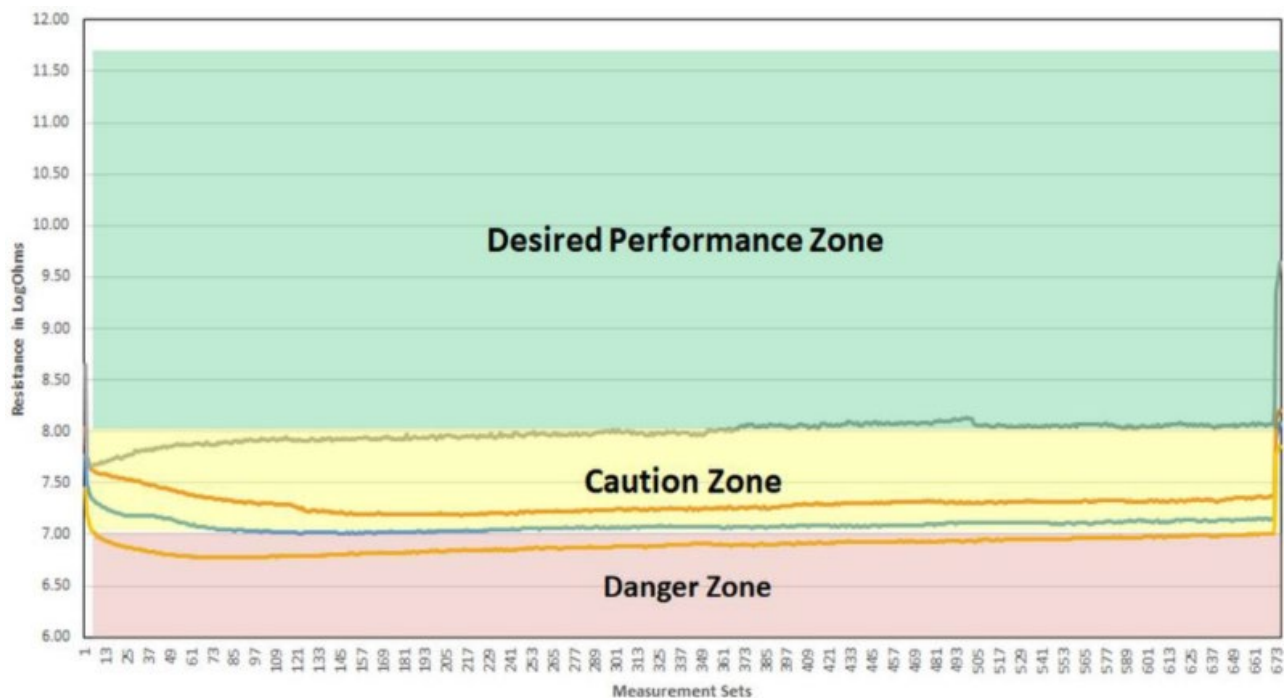


Figure 6: SIR Performance Zones Defined

SnPb SP #1: Not Cleaned

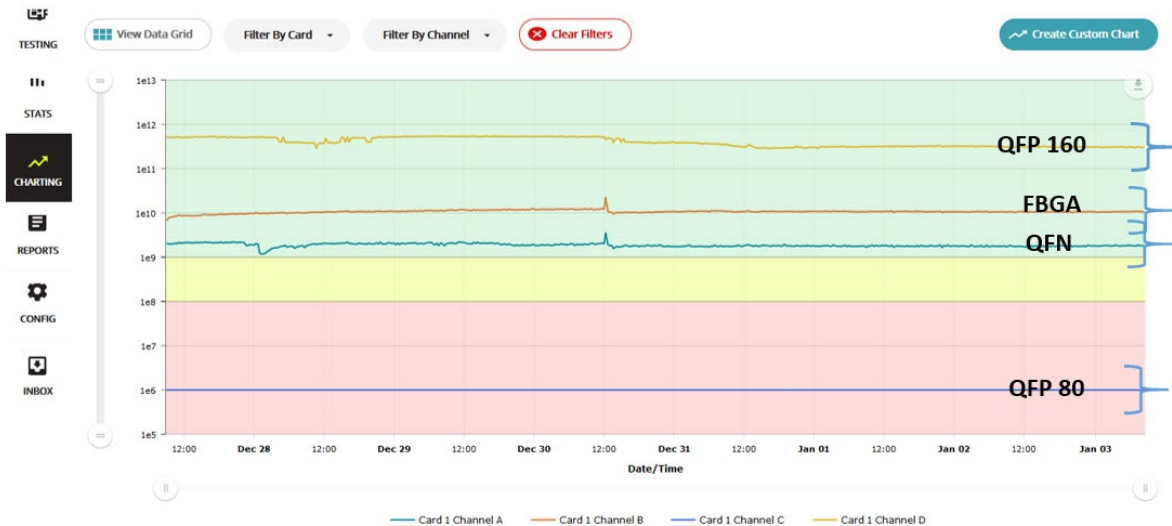


Figure 7: SnPb Solder Paste #1 Not Cleaned

Solder Paste #1 represents a tin-lead high-reliability no-clean product. The QFP-160 is a leaded component with 160 leads with a 0.65 mm pitch. During reflow, the flux component is not shadowed, which allows for proper outgassing and activator decomposition. The rosin/resin oxygen barrier encapsulates metal oxides that resists moisture. As a result, the SIR values exceed 11 logQs. When considering the FBGA with the center lug and 1 mm pitch, the standoff height is in the range of 254µms (10 mils). Similar to the QFP-160, the standoff gap allows for adequate heat transfer and flux outgassing. The SIR values are a decade lower than the QFP-160, which could be due to the center lug. The QFN component has challenging features. The center lug and 0.5 mm pitch equate to a high level of solder mass. The low standoff in the range of 25-50µms reduces proper outgassing during reflow. The flux residues under the QFN are more active, resulting in SIR values over 2 decades lower.

SnPb SP #2: Not Cleaned



Figure 8: SnPb Solder Paste #2 Not Cleaned

SnPb Solder Paste #2 is more active than Solder Paste #1. The QFN component is now in the danger zone.

Pb-Free SP #3 – Not Cleaned

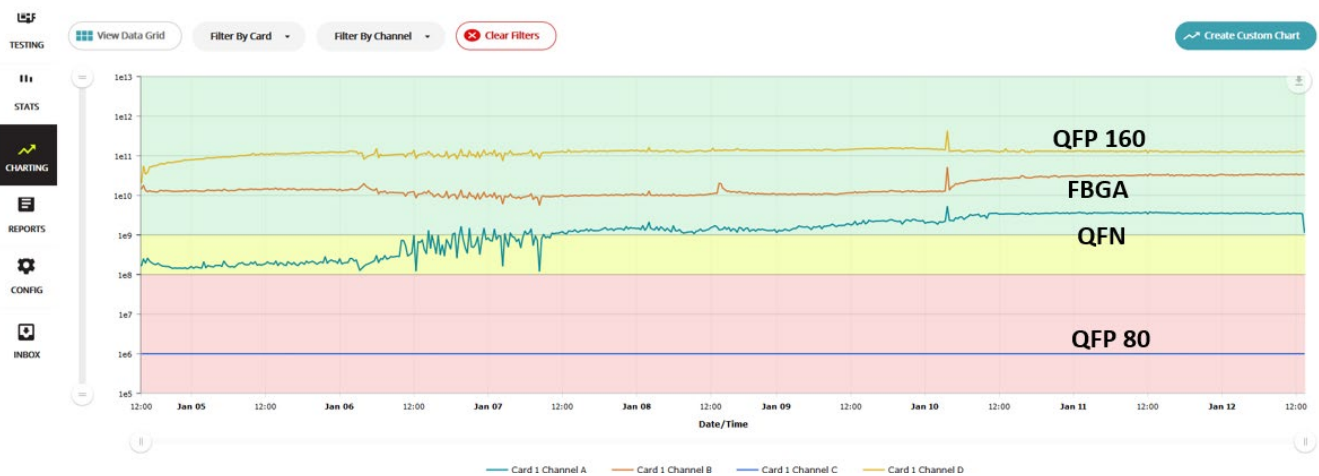


Figure 9: Pb-Free Solder Paste #3 Not Cleaned

The Pb-Free Solder Paste #3 shows a similar behavior as Solder Paste #1. The QFN values continue to be lower.

SnPb SP #1: QFN Cleanliness Comparison

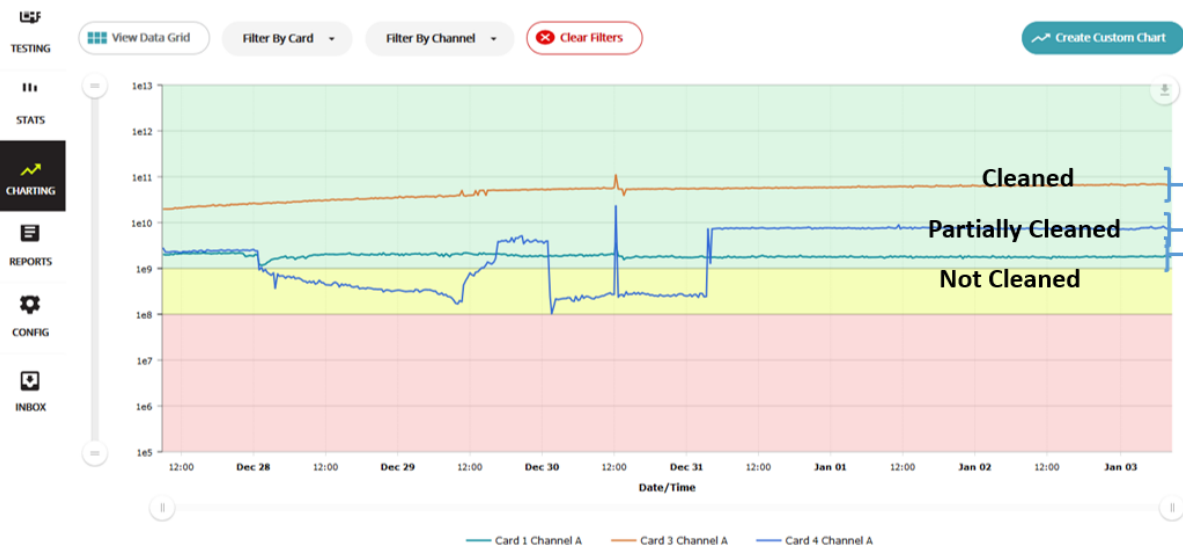


Figure 10: SnPb Solder Paste #1 – QFN Cleanliness Comparison

Figure 10 provides insight into the Cleaning process. When the QFN is cleaned, the SIR values are over 2 decades higher. The concern is when errant residue is still present under the QFN post cleaning. The SIR values indicate that the errant residue is active. Dialing in the cleaning process to assure that the QFN is cleaned is an important criteria.

SnPb SP #2: QFN Cleanliness Comparison

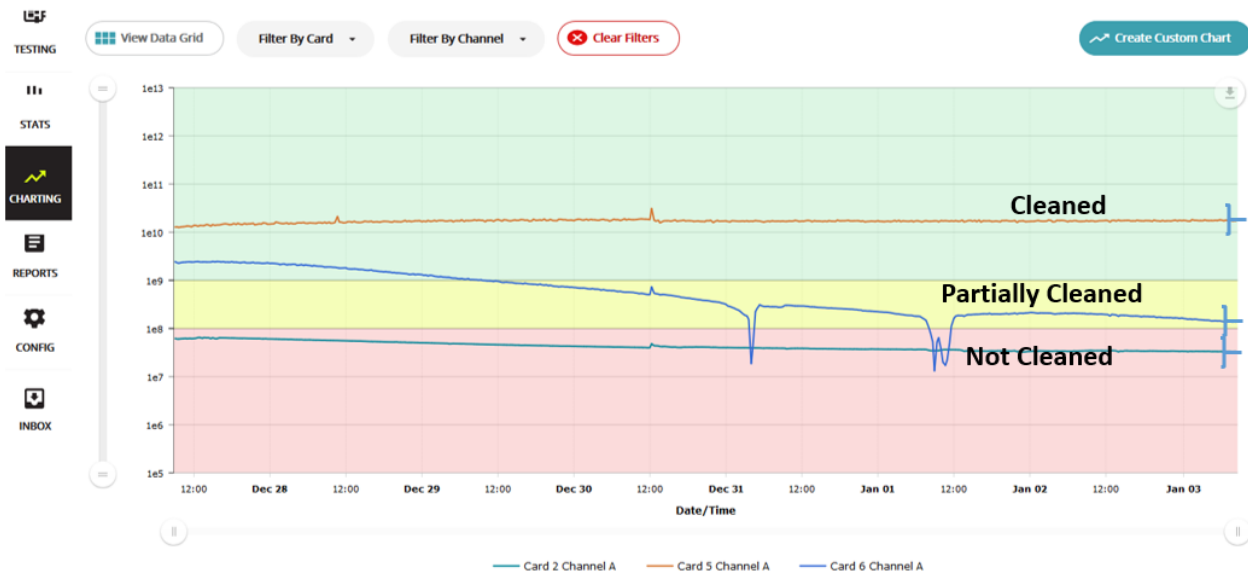


Figure 11: SnPb Solder Paste #2 – QFN Cleanliness Comparison

On solder paste #2, the activity level of this paste is apparent. If cleaned, the SIR values meet the desired criteria. If residue is left under the bottom termination post cleaning, the SIR values move into the danger zone.

Pb-Free SP #3 – QFN Cleaning Comparison

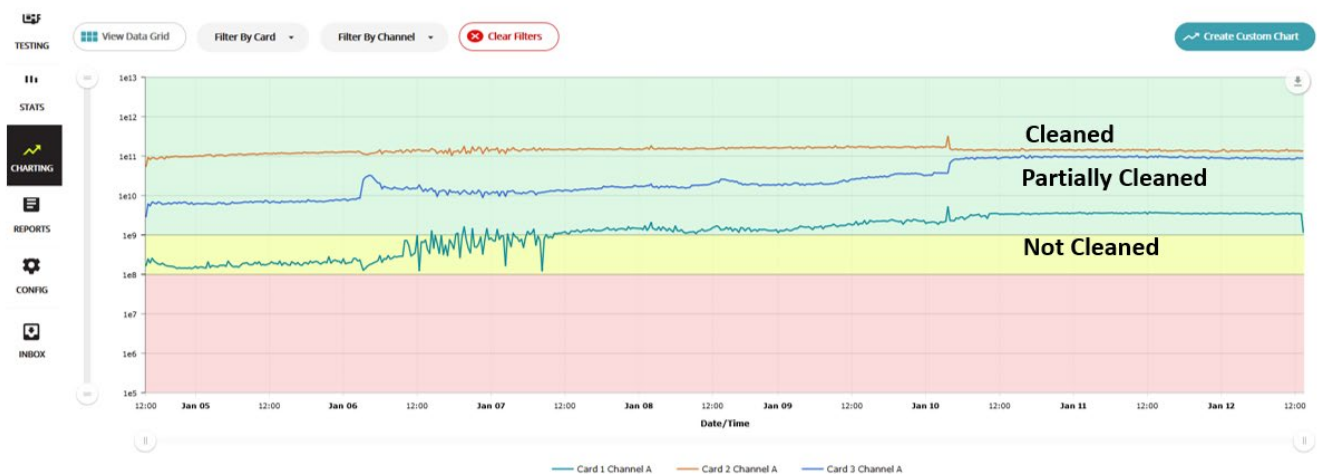


Figure 12: Pb-Free Solder Paste #3 – QFN Cleaning Comparison

SnPb #1: FBGA Cleanliness Comparison

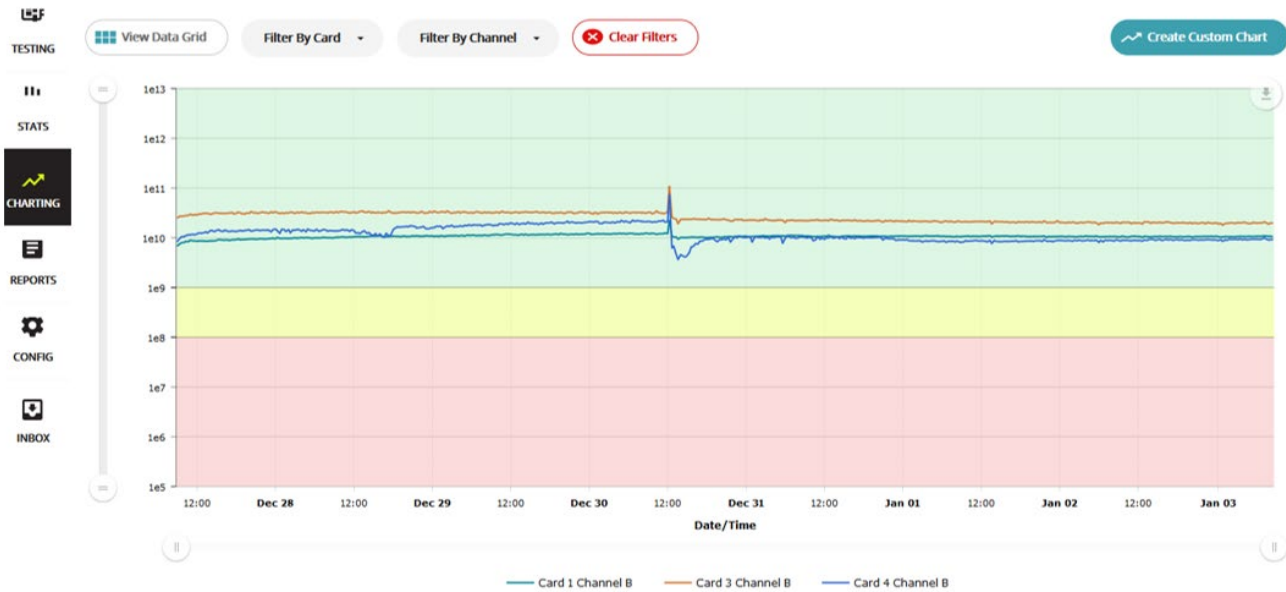


Figure 13: SnPb Solder Paste #1 – FBGA Cleaning Comparison

Notice the consistency on the FBGA component. The high standoff of roughly 254 μ m provides good outgassing. The component is easily cleaned resulting in SIR values in the desired range. Even for Not Cleaned boards, the SIR values are excellent.

SnPb SP #2: FBGA Cleanliness Comparison

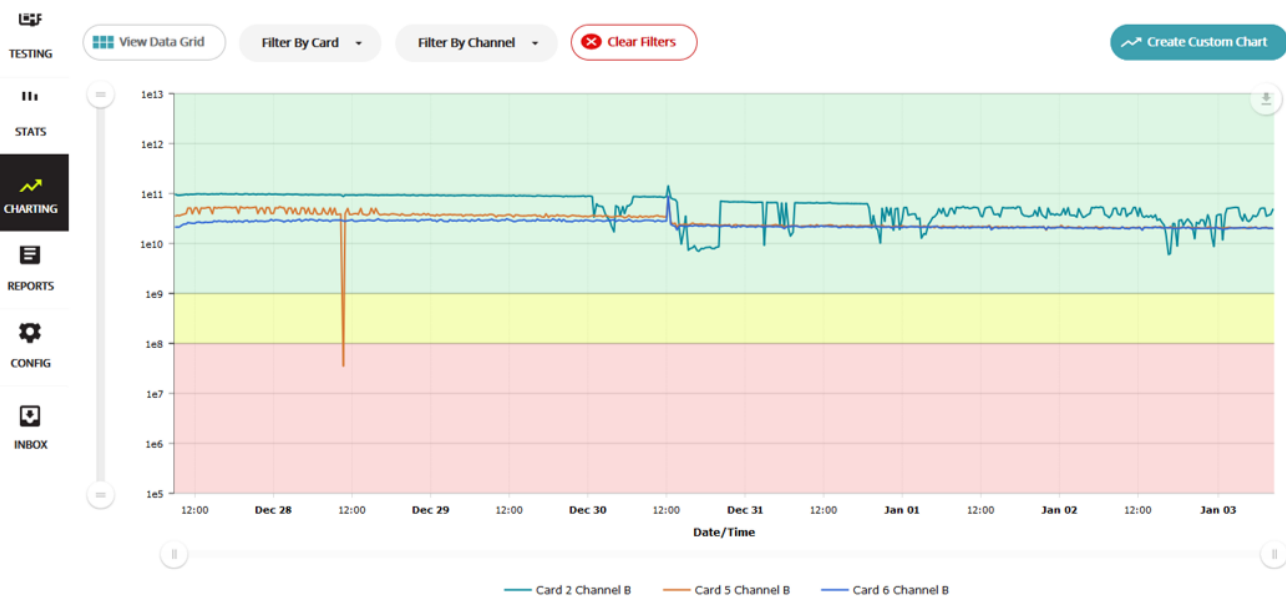


Figure 14: SnPb Solder Paste #2 – FBGA Cleaning Comparison

For solder paste #2, there is evidence of a leakage current event on the partially cleaned board, but with full recovery. The SIR values all range in the desired zone.

Pb-Free SP #3: FBGA Cleaning Comparison

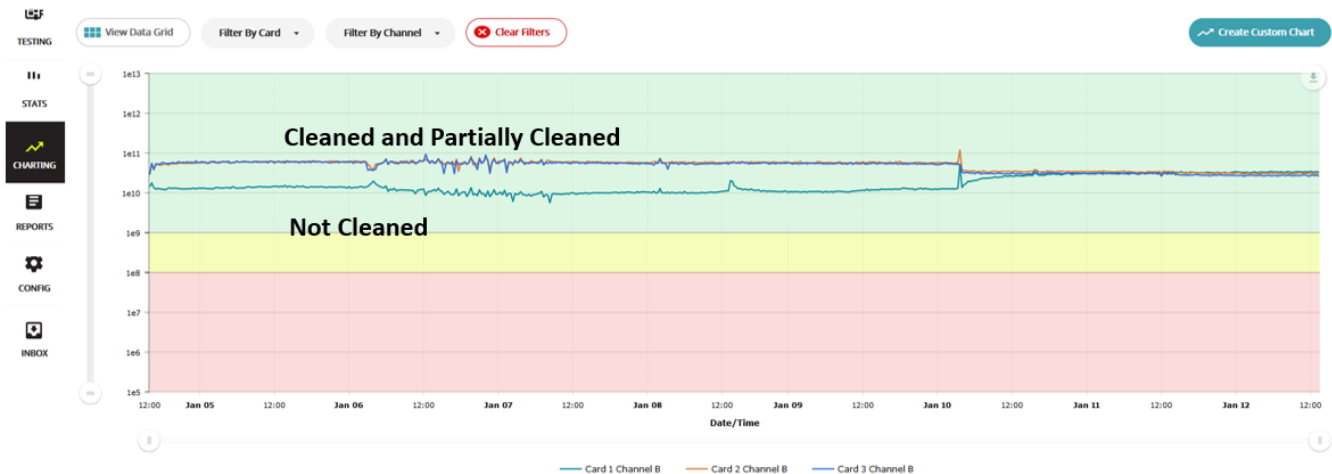


Figure 15: Pb-Free Solder Paste #3 – FBGA Cleaning Comparison

The Pb-Free solder paste #3 shows consistency on the FBGA regardless of the cleaning condition.

SnPb SP #1: QFP 160 Comb Cleaned Comparison

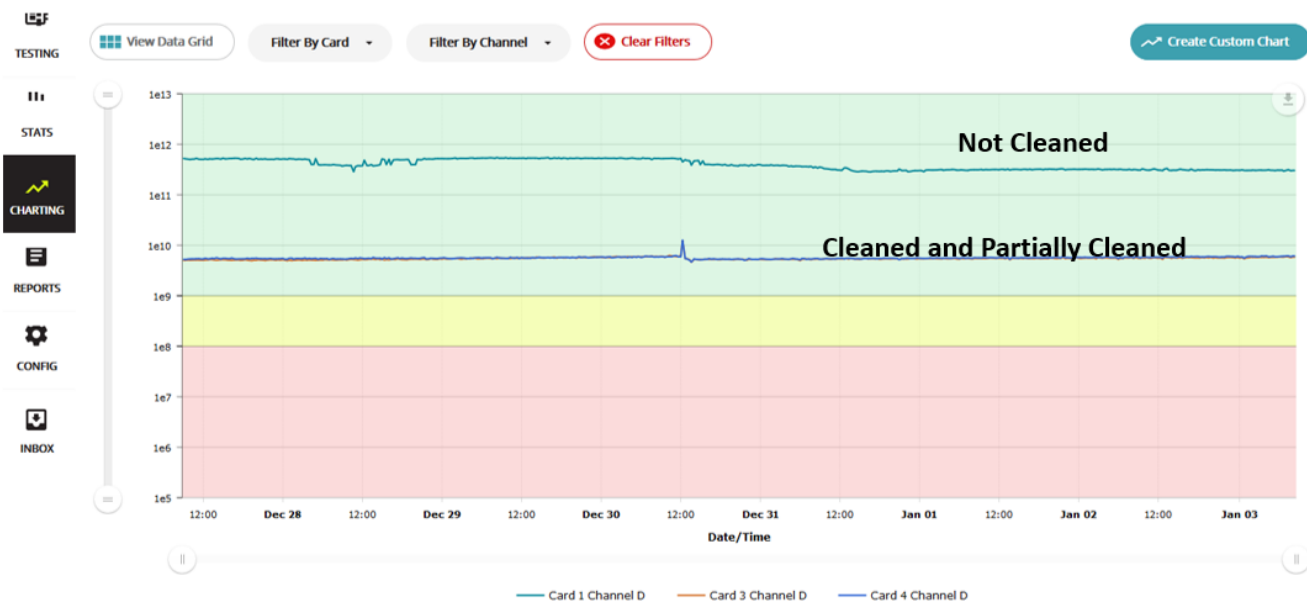


Figure 16: SnPb Solder Paste #1 – QFP-160 Cleaning Comparison

The QFP is a leaded component. When the flux component sees proper heat transfer and outgassing during reflow, the not cleaned residue is highly reliable. Both cleaned and partially cleaned residues were lower than the no-cleaned residue but still reliable.

SnPb SP #2: QFP160 Comb Cleaning Comparison

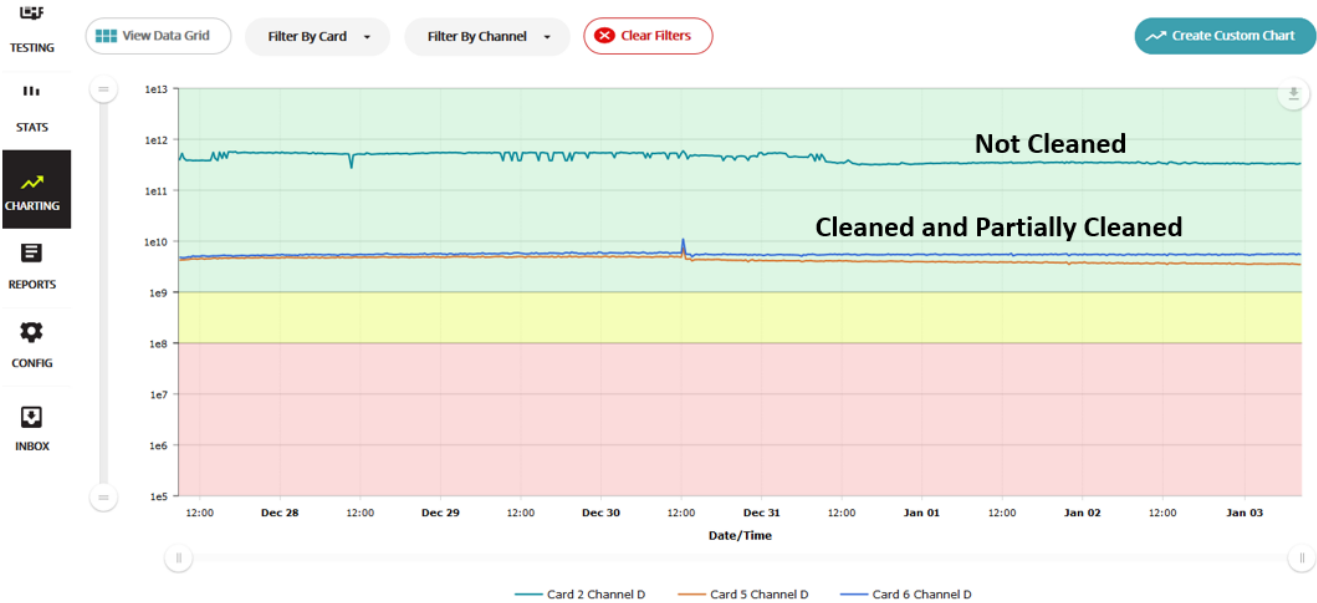


Figure 17: SnPb Solder Paste #2 – QFP-160 Cleaning Comparison

On the higher activity solder paste #2, the behavior on the QFP is similar to solder paste #1.

Pb-Free SP #3: QFP 160 Cleaning Comparison

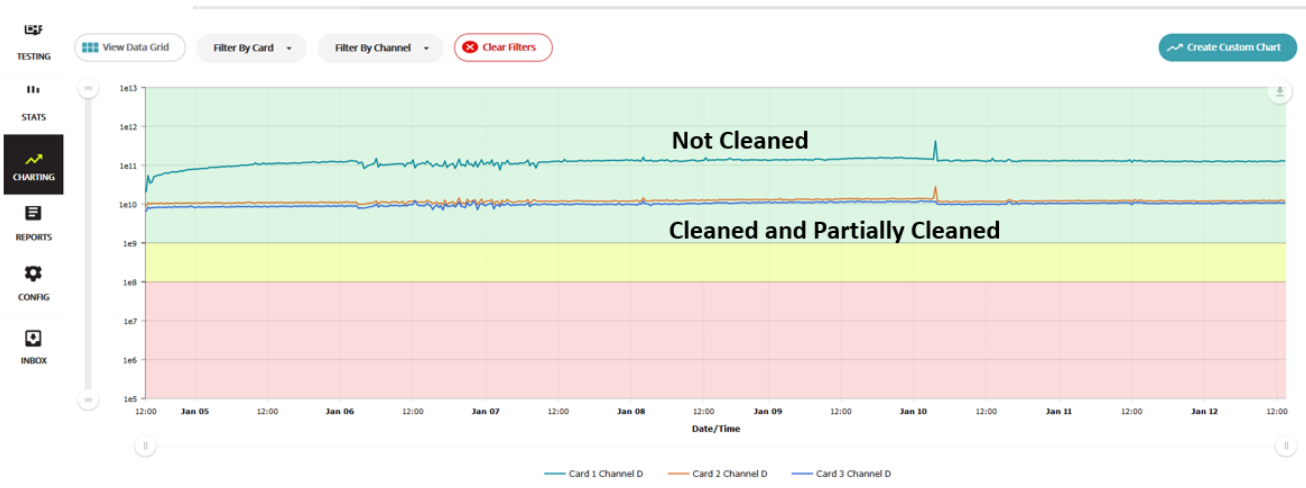


Figure 18: Pb-Free Solder Paste #3 – QFP 160 Cleaning Comparison

Step 2: Identify and analyze the risks associated with contamination left on the device from all potential sources

The green area in the chart is the desired performance zone. The range was set at $9 \log\Omega$. The yellow area ($8 \log\Omega - \log 9 \Omega$) is considered the cautionary zone. The red area is considered (below $8 \log\Omega$) the danger zone.

For the three solder pastes tested, the QFP 80 (Channel C) showed a direct short during the testing process. The cause for this failure was component related. The QFP 80 component had an active die and was not a dummy component, which is required for testing.

The solder pastes selected for this study are rated as Low Residue No-Clean solder pastes. A No-Clean solder paste reduces the residue level. Weak organic acids comprise the

activators used within these No-Clean solder pastes. The activators are designed to decompose during the reflow process. Any remaining flux residue is intended to encapsulate metal oxides within a resin shell. To meet the No-Clean standard, the material must pass both SIR and Ion Chromatography levels as specified in IPC J-STD-004.

The SIR test method showed differences based on the solder paste, component and cleaning condition. The resistivity values for the QFP-160 component were either in the range or higher than 11 logΩs. The soldered area on the QFP-160, located on the periphery, provides proper heat exposure during the soldering process. The No-Clean solder paste for all three solder pastes leaves a benign residue on the QFP-160 component. The QFP-160 is at low risk of failure when exposed to harsh conditions.

The FBGA resistivity levels exceed 10 logΩs for the three No-Clean solder pastes tested. The FBGA component has a standoff gap of roughly 10 mils (254 μms). The 10 mil standoff provided ample area for the flux to properly outgas during reflow. Similar to the QFP-160, the flux residue left under the FBGA is at low risk of failure when exposed to harsh conditions.

The QFN resistivity levels were far different than those for the QFP-160 and FBGA components. The SnPb Solder Paste #2 QFN resistivity levels range in the 7–8 logΩs. SnPb Solder Paste #1 resistivity levels exceeded 9 logΩs. Solder paste #1 was at less risk on the QFN component. For the Pb-Free solder paste #3, the QFN component resistivity levels were also lower. The SIR test showed signs of leakage currents early in the test process. Four problem areas occur: 1.) Low standoff gap in the range of 1-2 mils (25-50μms); 2.) A large mass of solder is present under the bottom termination; 3.) During reflow, blocked flux outgassing channels render a more active flux residue; 4.) The flux residue under the component termination is wet and pliable allowing both activators and metal oxides to be dissolved in monolayers of moisture. The flux residue under the QFN on Solder Paste 2 & 3 show a risk of failure when exposed to harsh conditions.

Cleaning the assembly following the soldering process reduces the risk of failure on the QFN component. When cleaned, the resistivity levels improved to the range of 10-11 logΩs. On assemblies partially cleaned, the QFN showed a risk of failure when the part was not fully cleaned. We defined this as partial cleaning. Dialing in the cleaning process to determine the wash time needed to entirely clean is an essential factor that reduces the risk of failure under the QFN component.

Step 3: Implement control measures to eliminate risks or mitigate their effects

Surface Insulation Resistance (SIR) is the best method for material and process characterization. This method, due to lack of automation and designs to process many channels, has not been used at the production site. To design SIR instrumentation for the production environment requires the integration and simplicity of the hardware; test boards targeted to specific components; and user interface that processes the real data time. The test must be robust and straightforward so that a technician can perform the analysis. Additionally, it must be highly repeatable, real-time, provide trend data, SPC charts and reports at the end of the test. The review must produce a pass/fail result.

Test boards designed with components that are smaller and smaller allow the user to access cleanliness on the most challenges components built into their design. Using the designed SIR Instrument, this miniaturized leadless and bottom terminated component, representative of production hardware, enable the assembler characterize their process and material set. Surface Insulation Resistance testing designed for the production resolves the question of “how clean is clean enough” to produce reliable electronics.

The current IPC Standards suggest 168 hours of run time to perform and SIR test. When verifying and validating soldering and cleaning materials, the 168-hour test is the right course of action. For process control, the SIR test on specific components can be discerned in a matter of hours. If there is residue under parts, problematic SIR values will be detected soon after the test begins (Figure 18).

SnPb SP #2: QFN Cleanliness Comparison

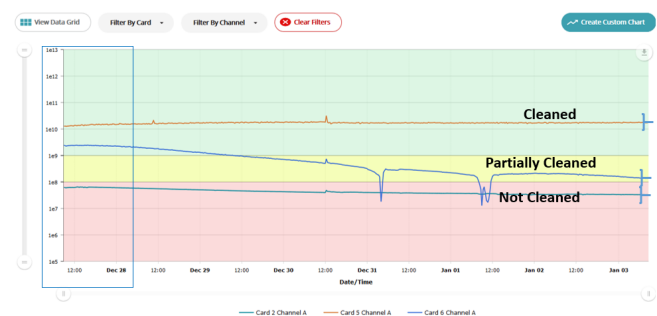


Figure 18: Using SIR for Process Control

Step 4: Monitor the effectiveness of these controls

SIR Instrumentation designed for the production floor allows for “Bottom-up Development.” The current approach requires the use of Ph.D.s and engineers to do the work and analysis. These guys are not going to catch problems or even diagnose them accurately every time. As a result, there is still a problem. Implementing SIR for process control provides the solution. The user-friendly and ease of use makes it less difficult to run the test. Due to the new system interface, real-time data analytics and trend data are

automatically done for the person on the floor. Eighty percent of the effort is done for the engineer.

The ability to test inside the production facility allow for process engineers to gain direct feedback of their choices. They can access material choices and process parameters and measure these values to build quality hardware. The result is objective evidence, statistical process control, and reliable and process repeatability.

CONCLUSION

The cleanliness of electronics manufactured by Class 3 segments is critical to reliability. Miniaturized IC, leadless and bottom terminated components trap active flux residues under the bottom termination. A risk management plan assures that Class 3 manufacturers both understand the problem, and employ methods to characterize solder and cleaning steps. On-going reliability testing using SIR provides the cleanliness information Class 3 manufactures need to know to develop process conditions that assure reliable electronics.

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REFERENCES

1. ReliaSystem (2019). RAM and Safety Assurance services for Aerospace. Retrieved from <http://www.reliasystem.com/aerospace-defence.html>
2. Qin, J, et al. (2005). Reliability Analysis of Avionics in the Commercial Aerospace Industry. University of Maryland, College Park.
3. Ernst & Young, LLP (2018). The 10 Risks in Aerospace & Defense. Retrieved from <https://www.ey.com/Publication/vwLUAssets/ey-top-10-risks-in-aerospace-and-defense/%24File/ey-top-10-risks-in-a&d.pdf>
4. Goertz, R.A. (1989). A guide to quality assurance indicators for the Defense Electronics Industry. United States Airforce.
5. Deloitte (2018). 2018 Global aerospace and defense industry outlook. Retrieved from
6. Deloitte (2019). 2019 Global Aerospace and Defense Industry Outlook. Retrieved from <https://www2.deloitte.com/content/dam/Deloitte>

</us/Documents/manufacturing/us-mfg-2019-global-a-and-d-sector-outlook.pdf>

7. Howard, C.E. (2008). Quality Control. Military & Aerospace Electronics. PennWell Corporation.
8. Zarr, R.F. (2018). The Future of High-Reliability Electronics. Retrieved from <https://www.electronicdesign.com/analog/future-high-reliability-electronics>
9. Parametric Technology Corporation (2011). Medical Device Reliability and Risk Management. White Paper. www.ptc.com
10. Northrup, M. & Rousseau, J. (2018). Is it time to retire ROSE Testing – Whether as a Cleanliness Test or Process Control Tool? emsnow.com
11. McMeen, M., Langley, C., Bixenman, M., & Lober, D. (2018). SIR Characterization of No-Clean Flux Residues under the QFN Component using Different PCB Board Design Options. SMTAI, Rosemont, IL.
12. Tempo Automation (2018). 5 Tips for Developing PCBs for Aerospace Electronics. Retrieved from <https://www.tempoautomation.com/blog/5-tips-for-developing-pcbs-for-aerospace-electronics/>
13. Von Tils, V. (2006). Design Requirements for Automotive Reliability. Robert Bosch GmbH, Automotive Electronics.
14. DfR Solutions' Insights (2019). Unique reliability challenges presented by automotive electronics. Retrieved from <https://www.com/blog/unique-reliability-challenges-presented-by-automotive-electronics>
15. Northrup, M. & Rousseau, J. (2018, March). Is it Time to Retire ROSE Testing – Whether as a Cleanliness Test or Process Control Tool? emsnow.com
16. Pauls, D., McMeen, M., & Bixenman, M. (2018). Development and Validation of an SIR-Based Process Evaluation System and Methodology. IPC/SMTA High Performance Cleaning and Coating Conference. Schaumburg, IL.
1. Sood, B. (2019). Focus on PCB Reliability to Drive Quality. IPC Reliability Forum. Baltimore, Maryland. IPC, Bannockburn, IL.
2. Karthik, V. (2019). No-Clean Solder Paste in Automotive Electronics – Enhanced Electrical Reliability in Harsh Environments. SMTA Electronics in Harsh Environments, Amsterdam, Netherlands. SMTA, Minneapolis, MN.

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