ELECTROCHEMICAL FAILURES AS A FUNCTION OF FLUX VOLUME UNDER BOTTOM TERMINATED COMPONENTS

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ABSTRACT
The activity of flux residue changes, when trapped under low profile leadless or bottom terminated components. There are three factors to consider: 1.) Standoff gap – Lower standoff gaps block outgassing channels. Low standoff gaps change the nature of the flux residue by leaving behind flux activators, solvents, and functional additives that normally would be outgassed from the residue. 2.) Narrow Pitch – Miniaturized components have a decreased distance between conductors of opposite polarity. There is a higher potential to bridge conductors with flux residue. 3.) Cubic Volume of Flux – Increased I/O in combination with thermal lugs creates a higher cubic volume of flux left under the bottom termination. High flux volumes can block outgassing channels and bridge conductors.

A QFN test board was designed to study the research hypothesis that electrochemical failure phenomena are related to the volume of flux residues present under the bottom terminated components. The designed test board (QFN-11) has four quadrants with varying mounting pad dimensions and component standoffs, resulting in varying amounts of flux volume. The test boards were evaluated using surface insulation resistance (SIR) methodologies, followed by visual analysis of the areas under the BTC components. An understanding of the relationship between flux volume and BTC pattern design is expected to aid assemblers in mounting pad design to reduce the risk of electrochemical failures.

Keywords: ECM, Dendrites, Parasitic Leakage, Bottom Terminated Components, QFNs, Cleanliness, J-STD-001G, Section 8

INTRODUCTION

Bottom Terminated Components trap process residues that can render electrochemical failures when exposed to harsh environments. Electronic hardware exposed to temperature extremes from a frost condition to high-temperature peaks exposes moisture to sensitive electronics. Flux residues that have not adequately outgassed are susceptible to electrochemical migration (dendrite growth).

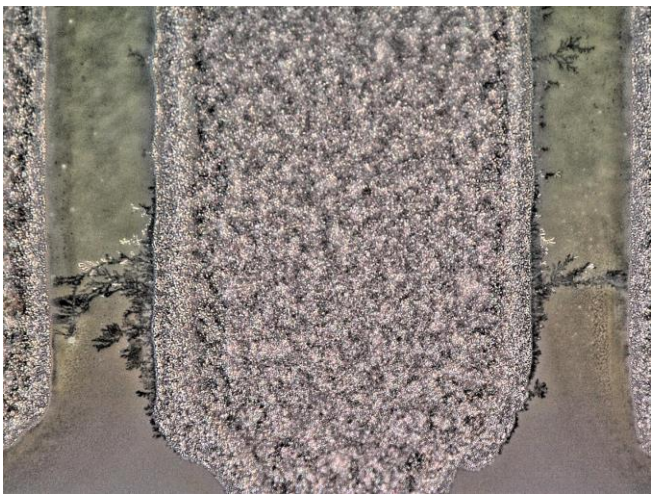

Figure 1: ECM in the path of Flux Residue

Surface Insulation Resistance (SIR) is the best test method for evaluating the electrochemical activity of soldering materials and process conditions.[1] The method quantifies harmful effects from solder flux and other process residues left on external surfaces after soldering.

Electrochemical reactions at or below the surface of electronic circuits will affect SIR.[2] These reactions are influenced by the presence of humidity, electrical bias, and ionic contaminations. SIR movement is a property of the flux material and electrode/bias system. The output represents the electrical resistance between two electrical conductors separated by some dielectric material. This property is loosely based on the concept of sheet resistances, but also contains elements of bulk conductivity, leakage through

electrolytic contaminants, multiple dielectric and metallization materials, and air.

Manufacturing process variables that can affect the properties of the materials system are numerous.

- Components – Leadless and Bottom Terminated Components are highly problematic due to the higher number of I/O, thermal lugs, and standoff gap.

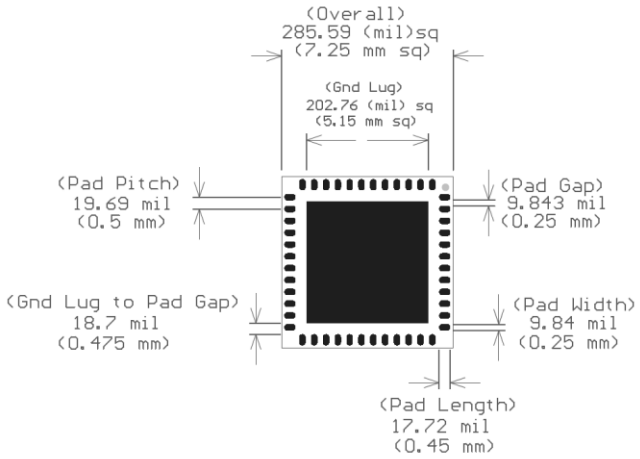

Figure 2: QFN 48 -11 Example

- Standoff Gap – Lower distance from the surface of the PCB to the component can block flux outgassing.
- Cubic Volume of Flux – Higher volumes of flux can bridge conductors. If the residue is pliable or active, there is a greater risk for ECM.
- Relative Humidity – Represents the amount of water vapor present in the air based on the temperature, which is comparable to the total amount of water the air can hold at that temperature.
- Voltage Gradient – The ratio of the applied voltage (expressed in volts) to the separation of electrodes (expressed in mm). Note: Contrary to Ohm's Law, the lower the voltage, the higher the propensity for dendrite formation.
- Bias Voltage – The electrical potential applied between adjacent connectors of a test pattern at all times when resistance measurements are not being made. For long-term characterization, the bias voltage should be chosen as representative of the voltages used on the final printed board assembly.
- Test Duration – The length of time the materials system is exposed to conditions other than ambient conditions.
- Thermal Cycling - The process of cycling through two temperature extremes, typically at relatively high rates of change. Thermal cycling is an environmental stress test used in evaluating product reliability as well as in manufacturing to catch early-term, latent defects by inducing failure through thermal fatigue.

PURPOSE OF THE RESEARCH

Three critical factors require consideration when factoring in the risk of flux residues trapped under component terminations.

1. Standoff Gap: Lower standoff gaps block outgassing channels. These blocked channels can leave active and pliable flux residues, which are a higher risk for electrochemical migration.
2. Narrow Pitch: The decreased distance between conductors increases the electrical field attraction for a positively charged metal oxide to migrate to negative cathode and plate back to the anode. There is also a higher risk of flux residue bridging conductors.
3. Cubic Volume of Flux: Tighter pitch, a higher number of I/O, and large thermal ground planes increase the volume of flux that is left under the component termination.

The purpose of this research is to study the SIR on a No-Clean test board as a function of the cubic volume of flux residue. A SIR test board was designed with varying pitches between the signal pins. As the pitch narrows, the pad size increases. The researchers believe that larger pad dimensions will increase the cubic volume of flux left under the component termination. The research question we are trying to answer is – as the volume of flux increases, will the surface insulation resistance decrease due to electrochemical migration?

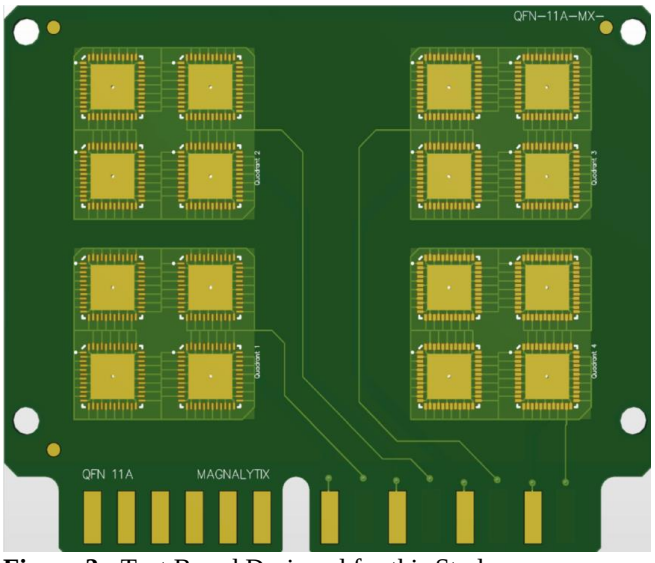

Figure 3 : Test Board Designed for this Study

The QFN test vehicle is a SIR test coupon for testing a Bottom Terminated (BTC) SMT style component that has bottom terminated I/O underside terminations. The objective

of this SIR test vehicle is to give the OEM or CM confidence that their reflow profile is achieving proper outgassing of the flux residues for no-clean fluxes and/or that the cleaning process has sufficiently cleaned the flux residue from underside of BTC style components.

The test board has four quadrants. Quadrant 1 is patterned with a 12-mil (304µm) gap/pitch with an 8-mil (203 µm) pad width. Quadrant 2 is patterned with a 10-mil (254 µm) gap/ pitch with a 10 -mil (254 µm) pad width. Quadrant 3 is patterned with an 8-mil (203 µm) gap/pitch with a 12-mil (304 µm) pad width. Quadrant 4 is patterned with a 6-mil (152 µm) gap /pitch with a 14-mil (355 µm) pad width. A glass slide replicate of the test vehicle was built to gain an understanding of the flux residue cubic volume under the component termination (Figure 4). The residue patterns are illustrated in Figures 5-8.

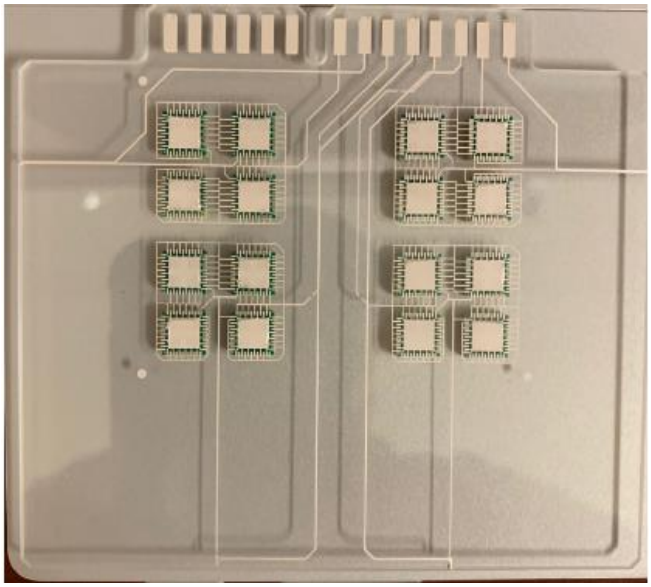

Figure 4: QFN Test Board built on a glass substrate to correspond to the exact PCB Test Vehicle of Figure 3

Quadrant 1 – QFN 48 - .5mm pitch – Non-Solder Mask Defined BTC with a ground lug for testing SIR under the component termination. The signal pins are patterned with a 12-mil (304µm) space with an 8-mil (203µm) pad, which aids in outgassing space.

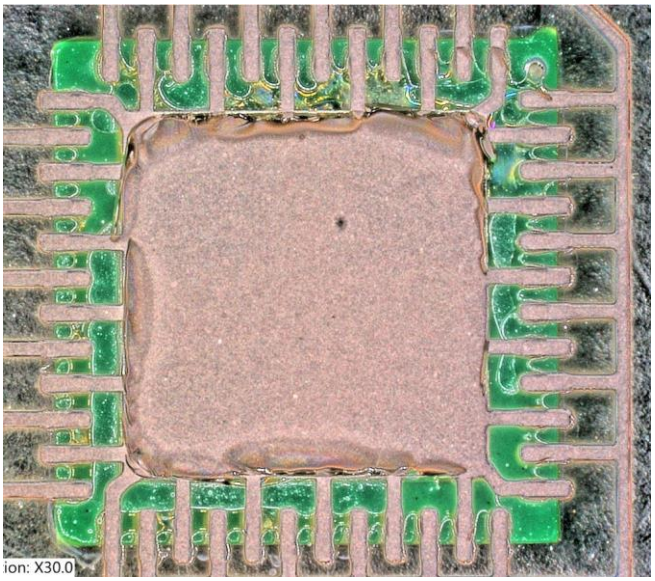

Figure 5: Quadrant 1 Flux Residue Pattern

Quadrant 2 – QFN 48 - .5mm pitch – Non-Solder Mask Defined BTC with a ground lug for testing SIR under the component termination. The signal pins are patterned with a 10-mil (254µm) space with a 10-mil (254µm) pad, which aids in solderability but slightly reduces outgassing over Quadrant 1.

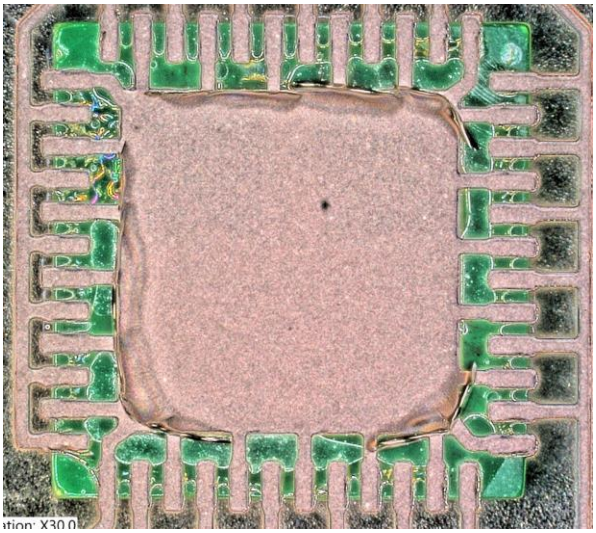

Figure 6: Quadrant 2 Flux Residue Pattern

Quadrant 3 – QFN 48 - .5mm pitch – Non-Solder Mask Defined BTC with a ground lug for testing SIR under the component termination. The signal pins are patterned with an 8-mil (203µm) space with a 12-mil (304µm) pad which aids in solderability but reduces outgassing over Quadrant 2. Figure 7B shows a dendritic short that migrated within the flux residue bridging the two conductors.

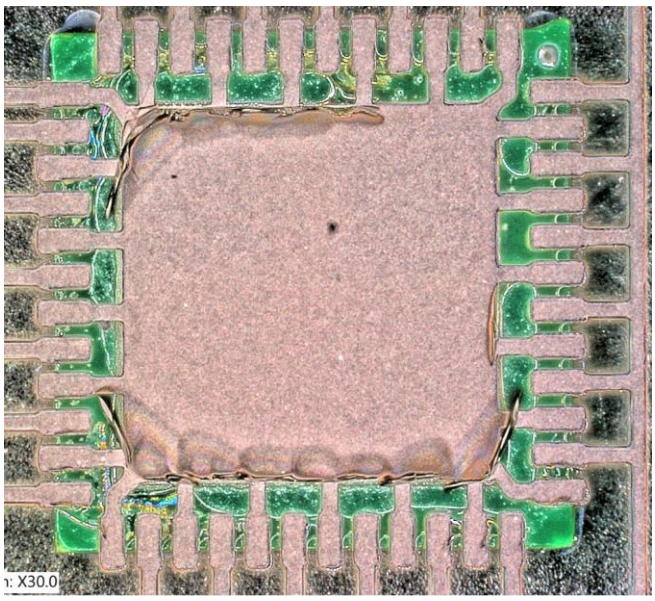

Figure 7A: Quadrant 3 Flux Residue Pattern

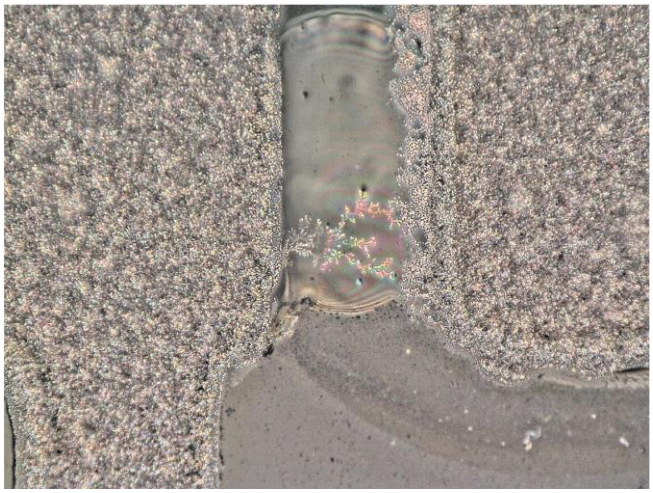

Figure 7B: Dendrite Short within Flux Residue

Quadrant 4 – QFN 48 - .5mm pitch – Non-Solder Mask Defined BTC with a ground lug for testing SIR under the component termination. The signal pins are patterned with a 6-mil (152µm) space with a 14-mil (355) pad, which aids in solderability but reduces outgassing over Quadrant 3.

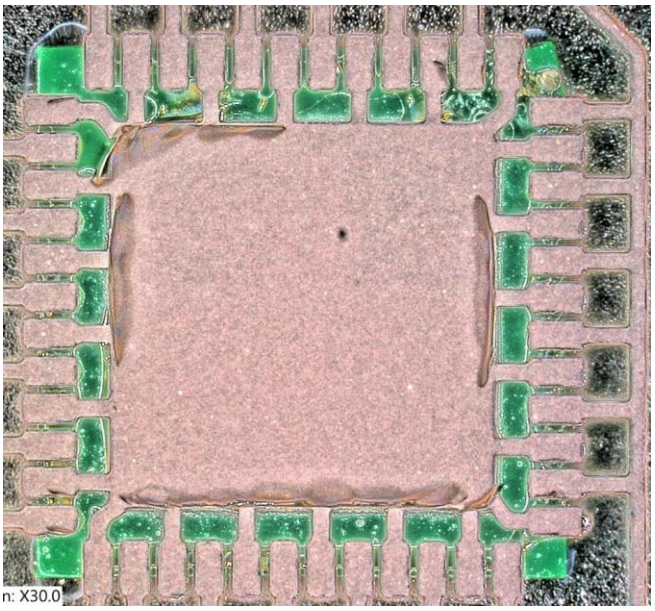

Figure 8: Quadrant 4 Flux Residue Pattern

The researchers believe the larger pad with reduced pitch will leave a higher cubic volume of flux under the component termination. From a design rule perspective, the variance of pad dimensions and pitch may provide insight into the risk of electrochemical failures due to the volume of flux trapped under the component termination.

EXPERIMENTAL

The test boards, shown in Figure 3, were assembled with a No-Clean solder paste. The test boards were SIR tested. Following SIR testing, the components were sheared off each quadrant and imaged.

Test Board #1:

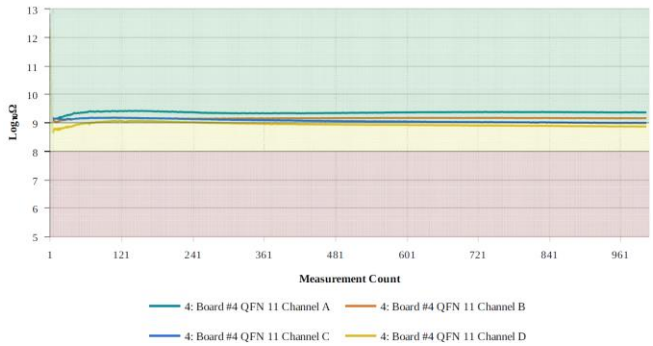

Figure 9: QFN Test Board #1

The No-Clean solder paste for Board #1 performed well. The insulation resistance was slightly lower as the pad size increased, and the pitch decreased. The resistance values in Table 1 reflect this trend.

Table1: Board #1 Stats

Board #1				
Measurement Stats	Channel A	Channel B	Channel C	Channel D
Maximum	9.422901 $Log_{10}\Omega$	9.191211 $Log_{10}\Omega$	9.18932 $Log_{10}\Omega$	9.068211 $Log_{10}\Omega$
Minimum	9.130649 $Log_{10}\Omega$	9.032823 $Log_{10}\Omega$	8.992033 $Log_{10}\Omega$	8.750143 $Log_{10}\Omega$
Median	9.370642 $Log_{10}\Omega$	9.164556 $Log_{10}\Omega$	9.052640 $Log_{10}\Omega$	8.926778 $Log_{10}\Omega$
Mean	9.364259 $Log_{10}\Omega$	9.160787 $Log_{10}\Omega$	9.070810 $Log_{10}\Omega$	8.941727 $Log_{10}\Omega$
Standard Deviation	0.035462 $Log_{10}\Omega$	0.017350 $Log_{10}\Omega$	0.057014 $Log_{10}\Omega$	0.059705 $Log_{10}\Omega$
Variance	0.001257 $Log_{10}\Omega^2$	0.000300 $Log_{10}\Omega^2$	0.003250 $Log_{10}\Omega^2$	0.003564 $Log_{10}\Omega^2$

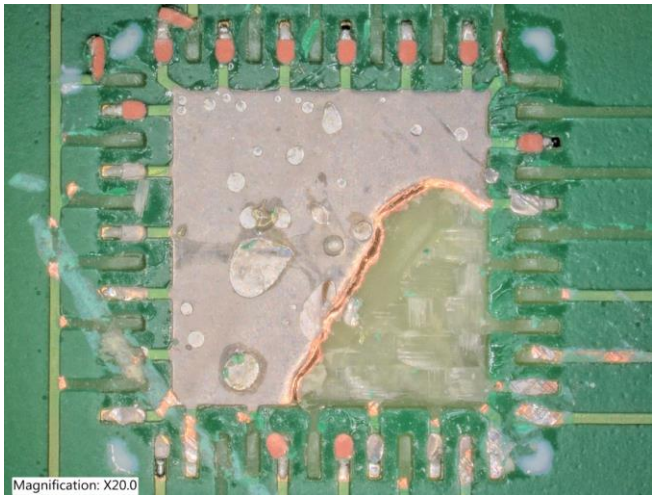

Figure 10: Quadrant #1 Board Side

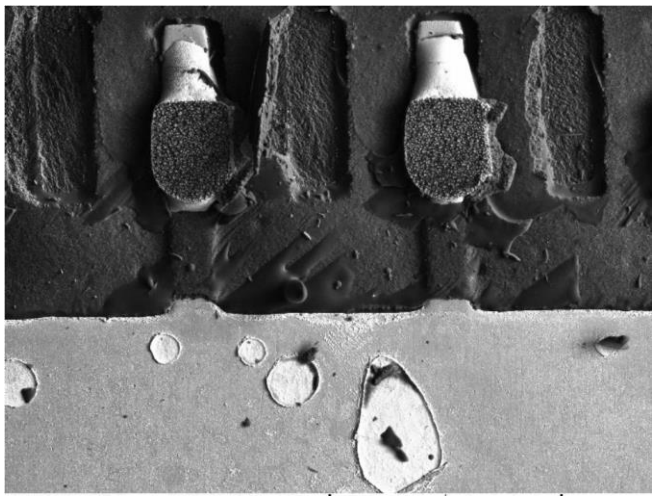

Figure 11: Quadrant 1 SEM Board Side 1

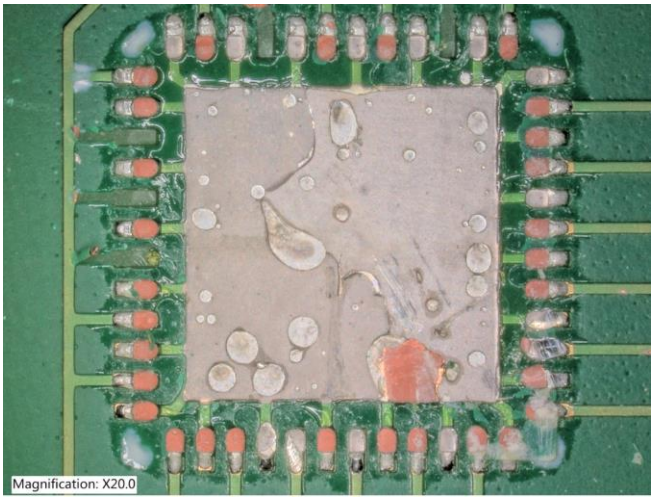

Figure 12: Quadrant 2 Board Side

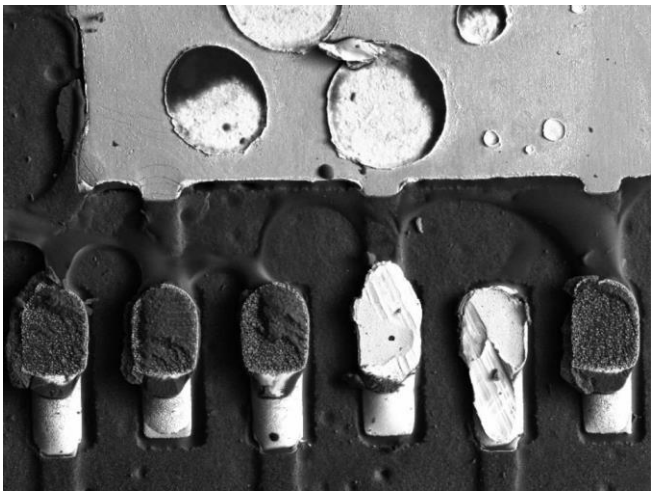

Figure 13 : Quadrant 2 SEM Board Side

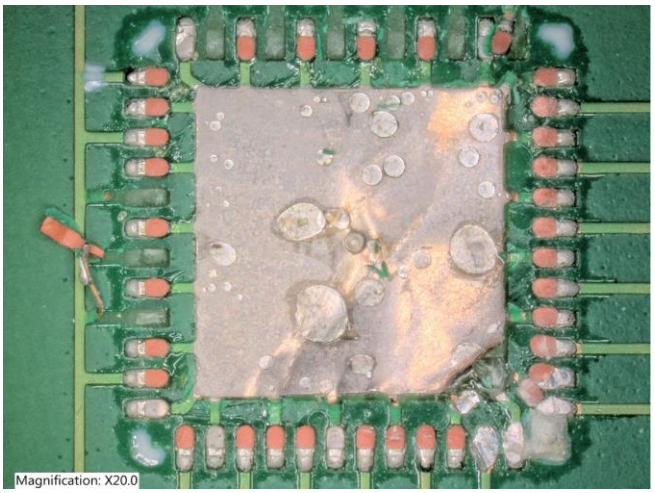

Figure 14 : Quadrant 3 Board Side

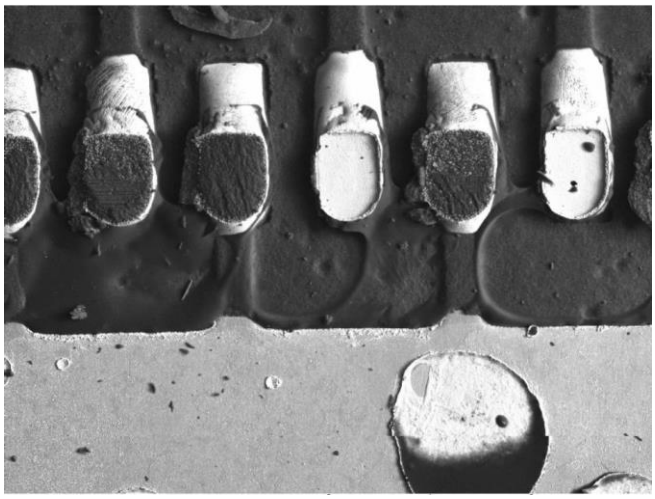

Figure 15: Quadrant 3 SEM Board Side

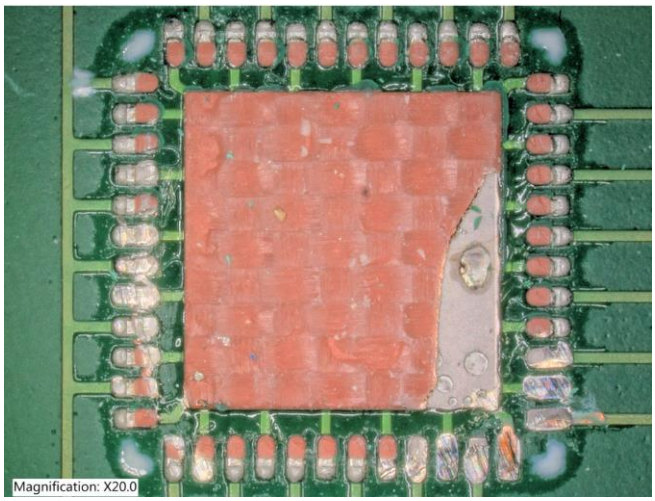

Figure 16: Quadrant 4 Board Side

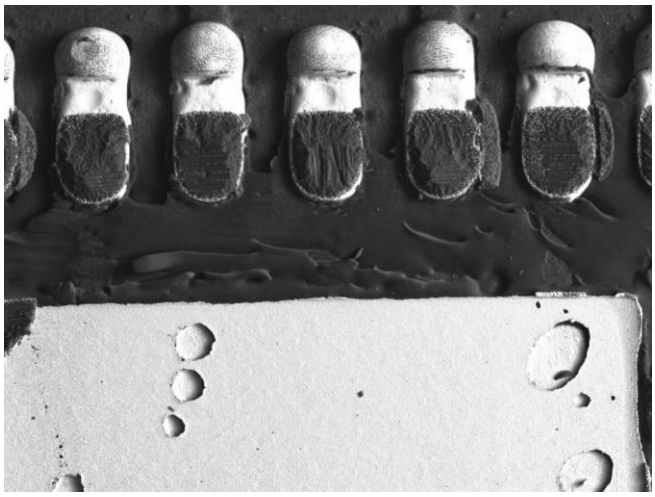

Figure 17: Quadrant 4 SEM Board Side

Test Board #2

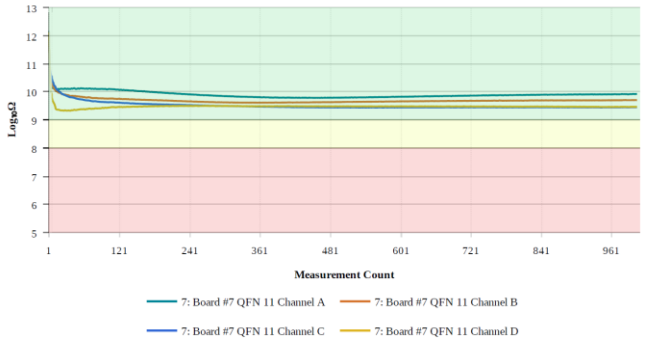

Figure 18: Board 2 SIR

The No-Clean solder paste for Board #2 also performed well. The insulation resistance was slightly lower as the pad size increased, and the pitch decreased. The resistance values in Table 2 reflects this trend.

Table 2: board 2 Stats

	Board #2			
Measurement Stats	**Channel A**	**Channel B**	**Channel C**	**Channel D**
Maximum	10.131383 $Log_{10}\Omega$	10.205428 $Log_{10}\Omega$	10.358668 $Log_{10}\Omega$	9.676312 $Log_{10}\Omega$
Minimum	9.779148 $Log_{10}\Omega$	9.609252 $Log_{10}\Omega$	9.436806 $Log_{10}\Omega$	9.320146 $Log_{10}\Omega$
Median	9.875354 $Log_{10}\Omega$	9.675059 $Log_{10}\Omega$	9.499899 $Log_{10}\Omega$	9.477014 $Log_{10}\Omega$
Mean	9.892748 $Log_{10}\Omega$	9.682835 $Log_{10}\Omega$	9.499899 $Log_{10}\Omega$	9.468274 $Log_{10}\Omega$
Standard Deviation	0.096138 $Log_{10}\Omega$	0.069404 $Log_{10}\Omega$	0.115251 $Log_{10}\Omega$	0.033716 $Log_{10}\Omega$
Variance	0.009242 $Log_{10}\Omega^2$	0.004816 $Log_{10}\Omega^2$	0.013282 $Log_{10}\Omega^2$	0.001136 $Log_{10}\Omega^2$

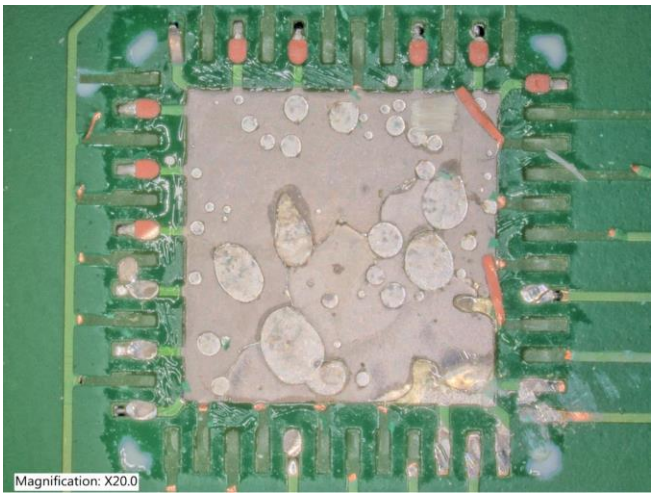

Figure 19: Quadrant 1 Board Side

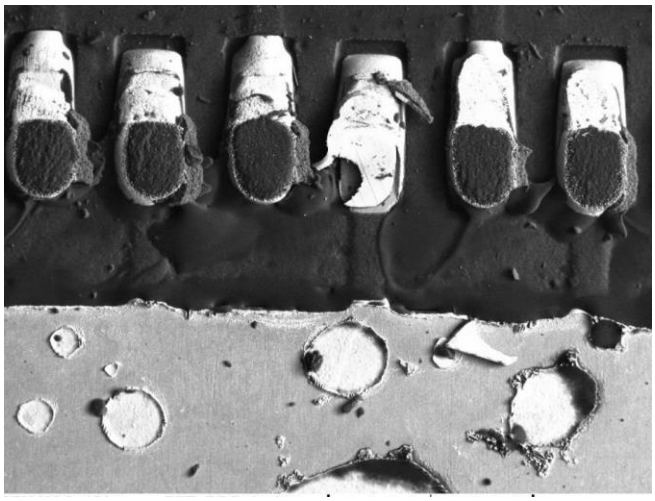

Figure 20: SEM Board Side

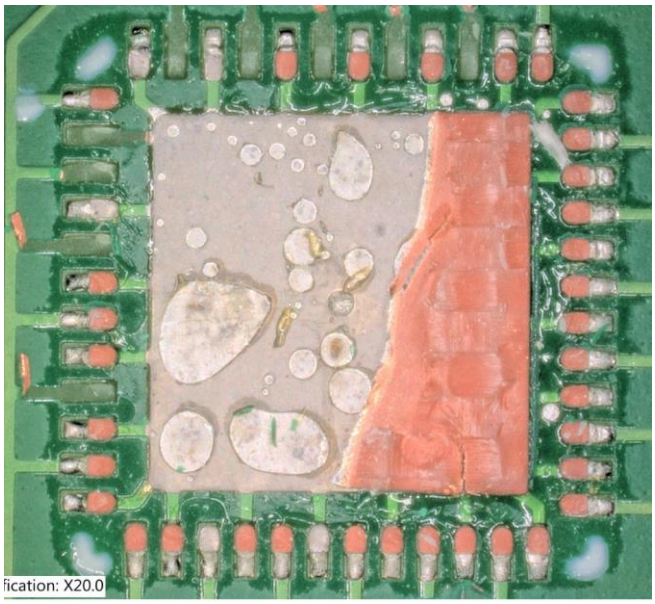

Figure 21 Quadrant 2 Board Side

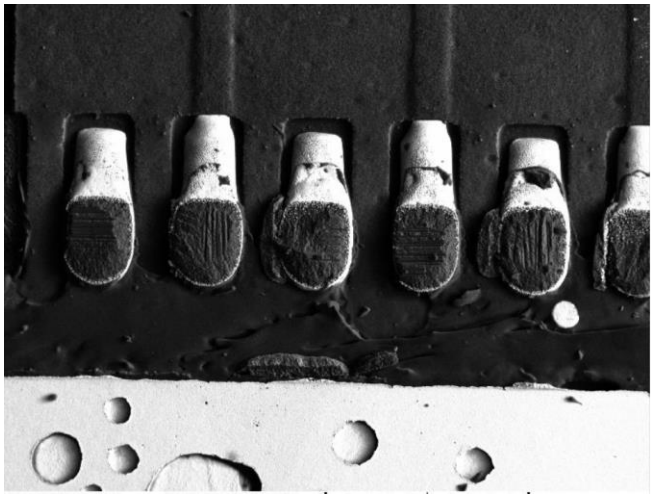

Figure 22: Quadrant 2 SEM Board Side

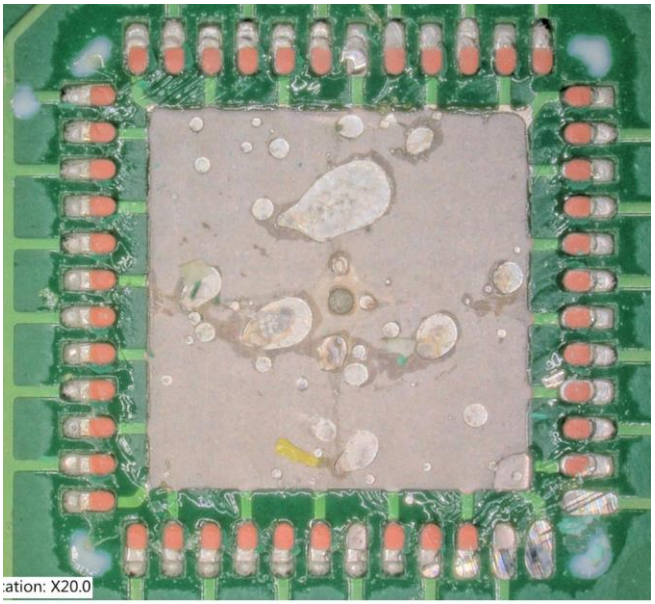

Figure 23: Quadrant 3 Board Side

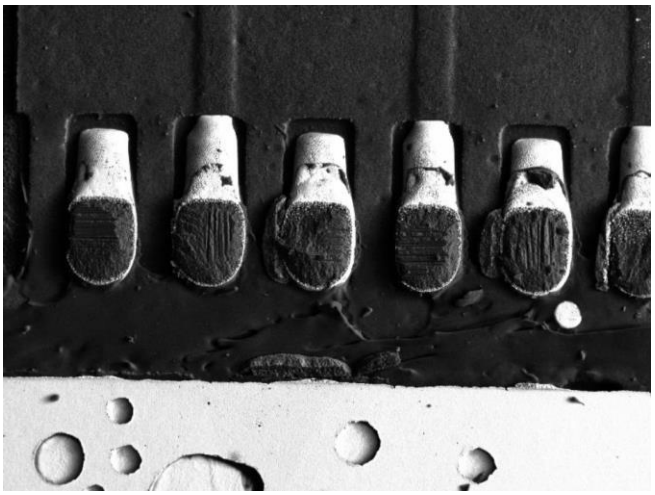

Figure 24: Quadrant 3 SEM Board Side

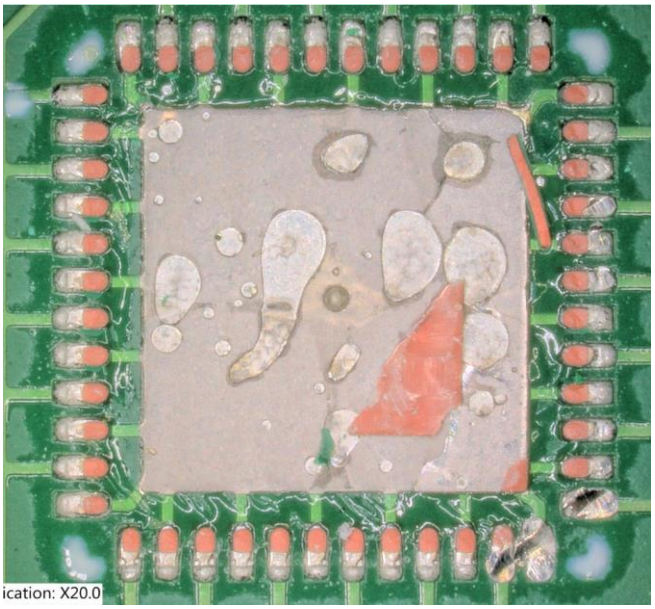

Figure 25: Quadrant 4 Board Side

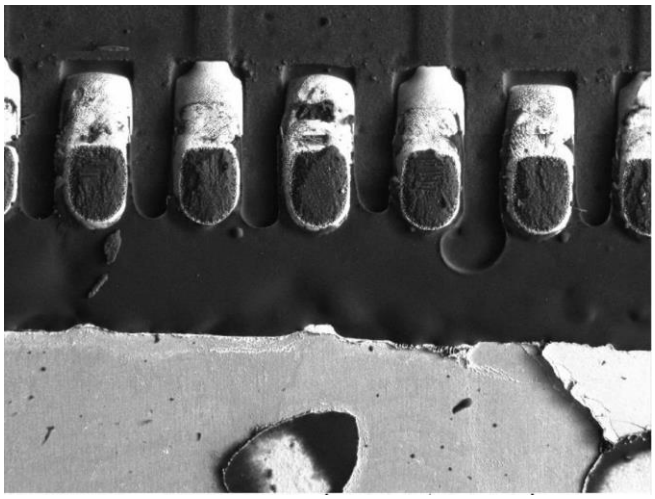

Figure 26: Quadrant 4 SEM Board Side

Test Board #3

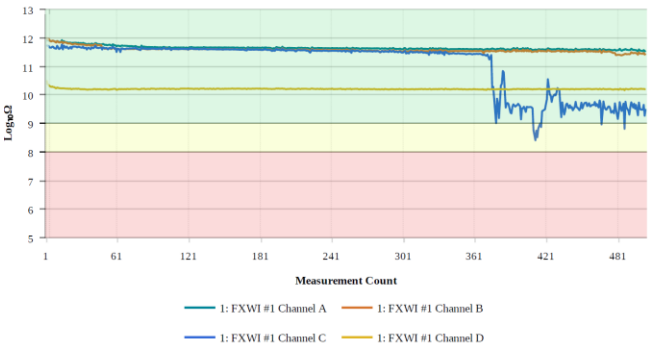

Figure 27: Board 3 SIR

The No-Clean solder paste for Board #3 exhibited insulation resistance at 12 $Log_{10}\Omega$s range. Channel C started to form parasitic leakage at the 360th measurement, which is roughly 120-hours into the test. The insulation resistance was slightly lower as the pad size increased, and the pitch decreased. The resistance values in Table 3 reflects this trend.

Table 3: Board 3 Stats

Board #3				
Measurement Stats	**Channel A**	**Channel B**	**Channel C**	**Channel D**
Maximum	11.915 $Log_{10}\Omega$	11.913 $Log_{10}\Omega$	11.762 $Log_{10}\Omega$	10.312 $Log_{10}\Omega$
Minimum	11.515 $Log_{10}\Omega$	11.381 $Log_{10}\Omega$	8.408 $Log_{10}\Omega$	10.159 $Log_{10}\Omega$
Median	11.630 $Log_{10}\Omega$	11.562 $Log_{10}\Omega$	11.531 $Log_{10}\Omega$	10.201 $Log_{10}\Omega$
Mean	11.643 $Log_{10}\Omega$	11.572 $Log_{10}\Omega$	10.045 $Log_{10}\Omega$	10.202 $Log_{10}\Omega$
Standard Deviation	0.069 $Log_{10}\Omega$	0.082 $Log_{10}\Omega$	0.885 $Log_{10}\Omega$	0.013 $Log_{10}\Omega$
Variance	0.004 $Log_{10}\Omega^2$	0.006 $Log_{10}\Omega^2$	0.783 $Log_{10}\Omega^2$	0.000 $Log_{10}\Omega^2$

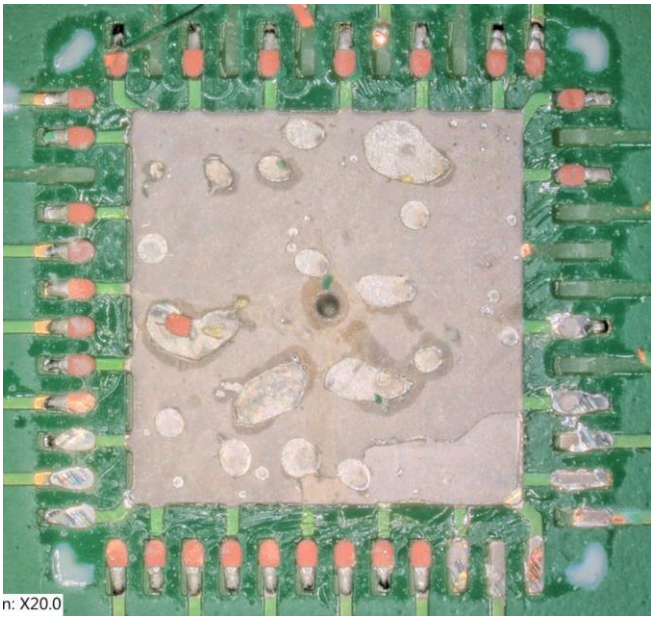

Figure 28: Quadrant 1 Board Side

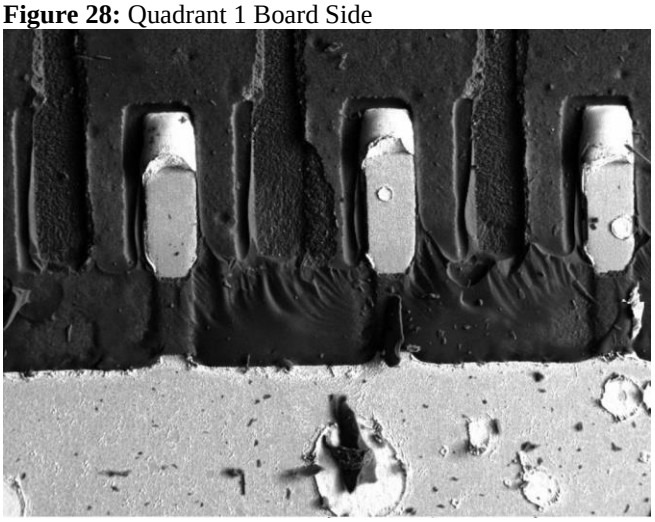

Figure 29: Quadrant 1 SEM Image

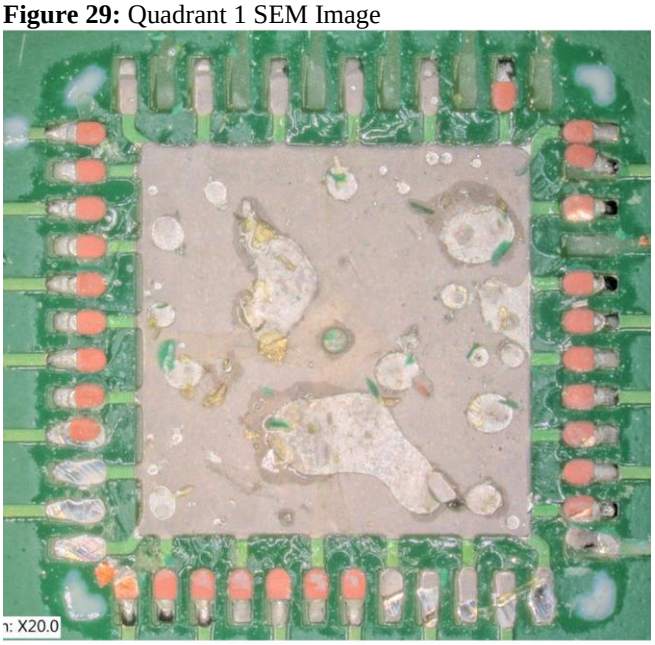

Figure 30: Quadrant 2 Board Side

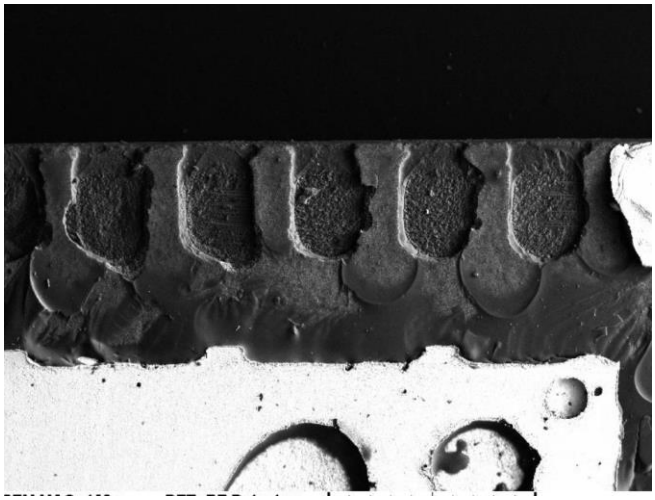

Figure 31: Quadrant 2 Board Side

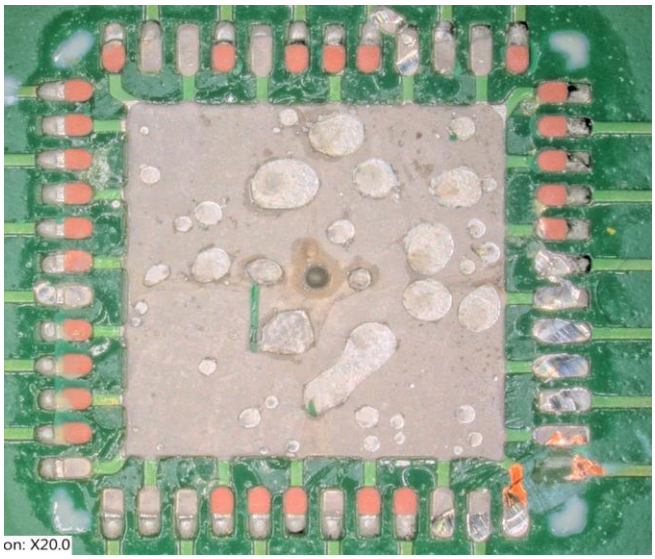

Figure 32: Quadrant 3 Board Side

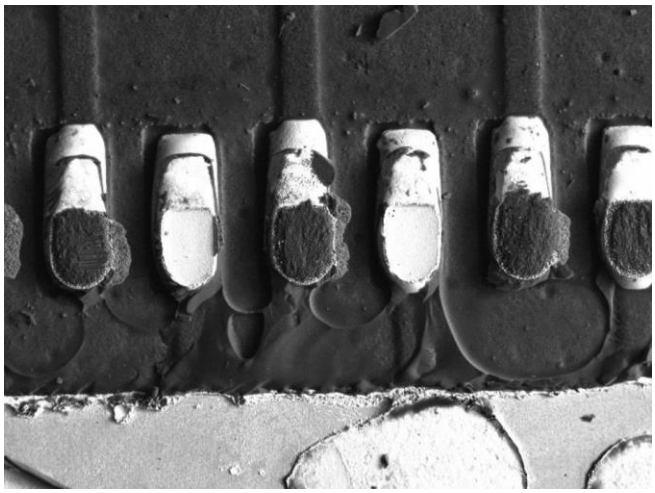

Figure 33: Quadrant 3 SEM Board Side

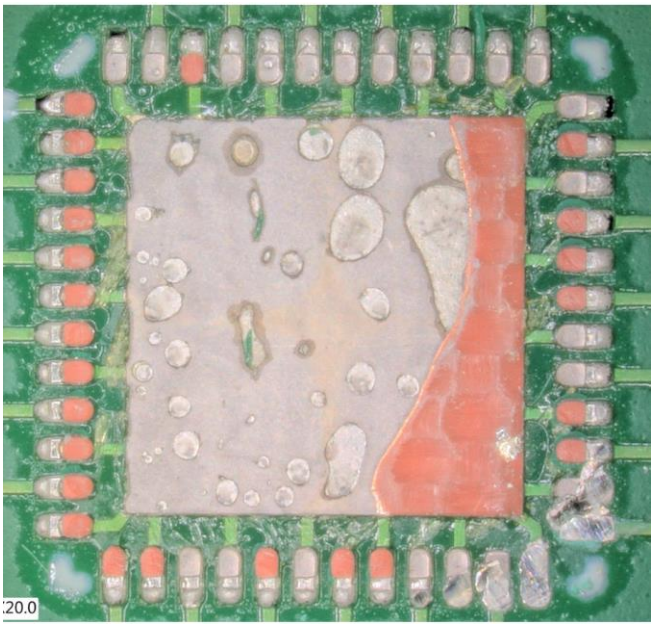

Figure 34: Quadrant 4 Board Image

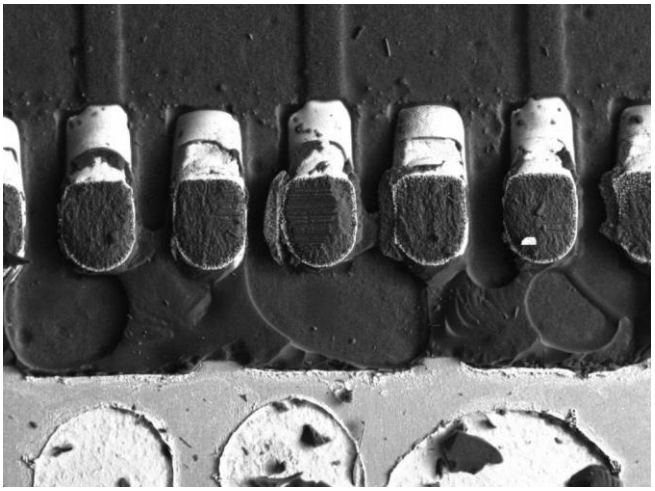

Figure 35: Quadrant 4 SEM Image

The SIR test on the QFN-11 test board in Figure 43 was soldered with a Water-Soluble solder paste and cleaned with DI water through an inline cleaning machine.

Test Board #4

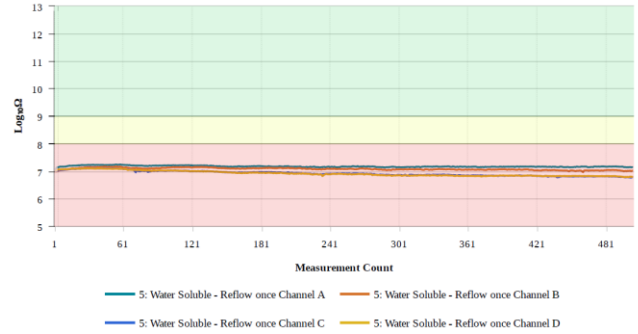

Figure 36: Water Soluble cleaned with DI using Inline

The Water-Soluble solder paste for Board #4 exhibited low insulation resistance across the four channels. These were cleaned but still exhibit residue under these bottom terminated components. The insulation resistance was slightly lower as the pad size increased, and the pitch decreased. The resistance values in Table 4 reflect this trend.

Table 4: Water Soluble cleaned with DI in an Inline Process

Board #4				
Measurement Stats	**Channel A**	**Channel B**	**Channel C**	**Channel D**
Maximum	7.148 $Log_{10}\Omega$	7.170 $Log_{10}\Omega$	7.113 $Log_{10}\Omega$	7.106 $Log_{10}\Omega$
Minimum	7.132 $Log_{10}\Omega$	6.968 $Log_{10}\Omega$	6.771 $Log_{10}\Omega$	6.789 $Log_{10}\Omega$
Median	7.170 $Log_{10}\Omega$	7.080 $Log_{10}\Omega$	6.914 $Log_{10}\Omega$	6.893 $Log_{10}\Omega$
Mean	7.178 $Log_{10}\Omega$	7.085 $Log_{10}\Omega$	6.924 $Log_{10}\Omega$	6.918 $Log_{10}\Omega$
Standard Deviation	0.025 $Log_{10}\Omega$	0.0399 $Log_{10}\Omega$	0.092 $Log_{10}\Omega$	0.093 $Log_{10}\Omega$
Variance	0.0006 $Log_{10}\Omega^2$	0.0015 $Log_{10}\Omega^2$	0.0085 $Log_{10}\Omega^2$	0.0086 $Log_{10}\Omega^2$

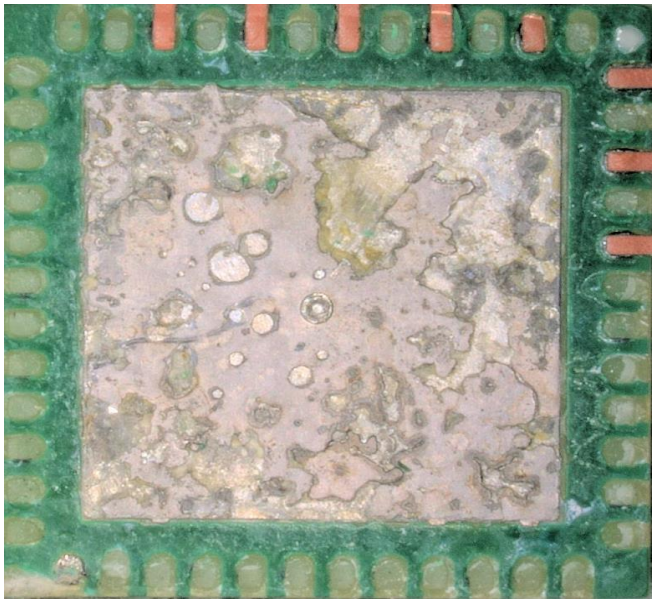

Figure 37: Quadrant 1 Component Side

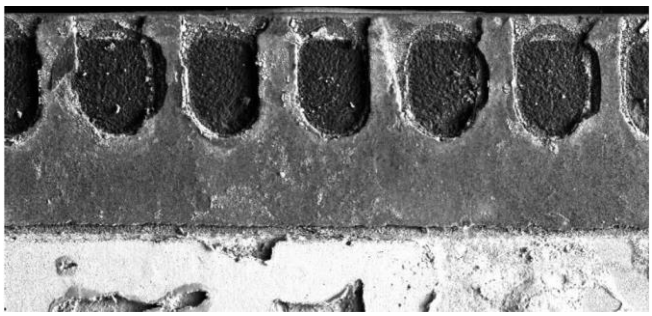

Figure 38: Quadrant 1 SEM Component Side

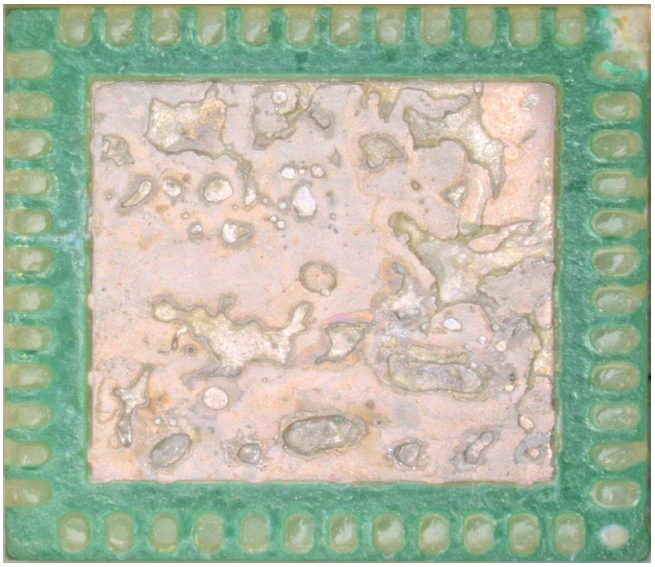

Figure 39: Quadrant 2 Component Side

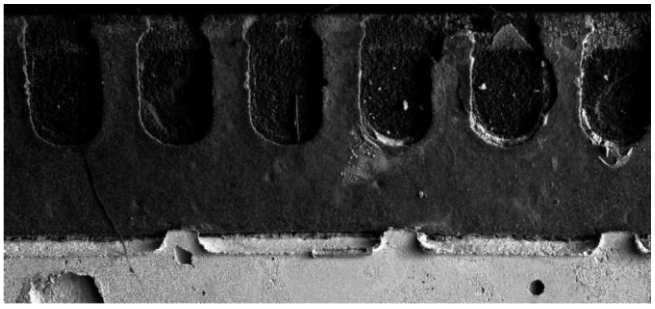

Figure 40: Quadrant 2 Component Side

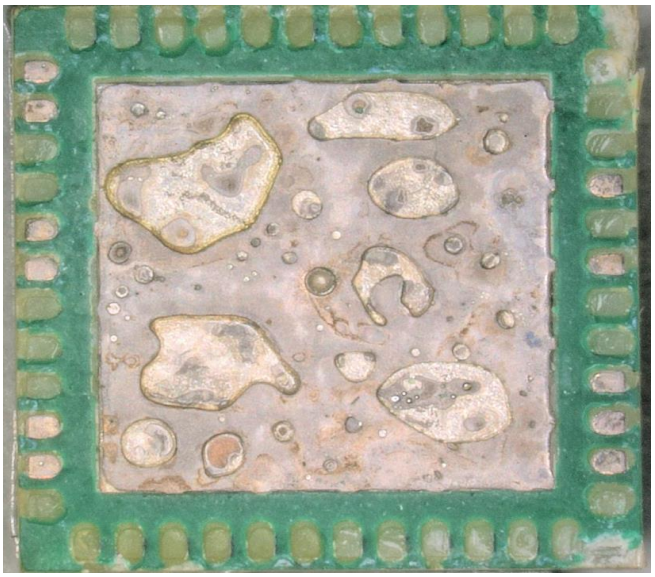

Figure 41: Quadrant 3 Component Side

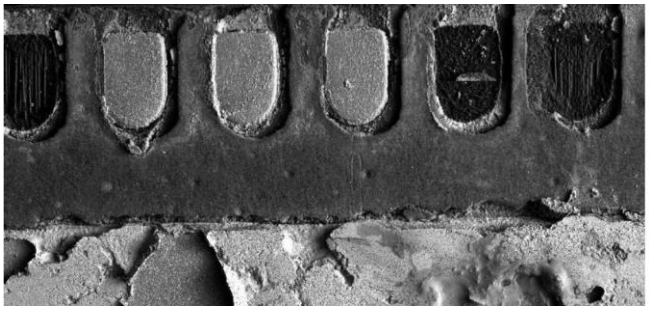

Figure 42: Quadrant 3 SEM Component Side

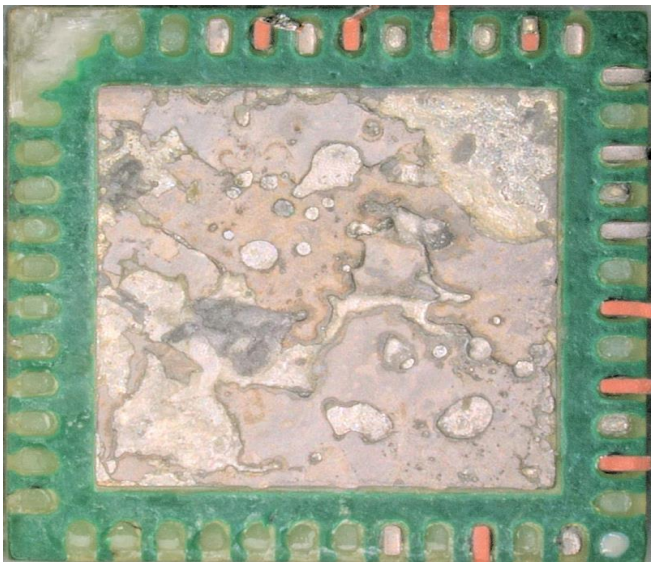

Figure 43: Quadrant 4 Component Side

Figure 44: Quadrant 4 SEM Component Side

INFERENCES FROM THE DATA FINDINGS

1. The glass slide test coupon allows one to see the flux residue in an uninterrupted state. The cubic volume of flux is a measureless number at this time. Still, one can visualize the change volumetrically between the ground lug and signal pins and also between the signal pins. As space / gap between the signal pins decreases, the cubic volume of flux is increasing and filling the available space or void between the ground lug and signal pins as well as filling the space between adjacent signal pins.
2. The No-Clean SMT paste used with the correct reflow profile and dwell times performed well in the testing of the new SIR test vehicle with almost all channels except for one which showed some parasitic leakage.
3. The mean SIR Values for the No-Clean SMT paste showed values ranging from 9 to 11 $Log_{10}\Omega s$, which shows the no-clean process has some degree of variability but the pass / fail criteria of 8 $Log_{10}\Omega s$ was met.
4. The QFN-48 SIR test vehicle showed the cubic volume of flux increased as the gap spacing between signal pins decreased, and the corresponding SIR drop that was expected. This was seen as a good correlation to the expected thesis.
5. The water-soluble SMT paste test also showed good consistent results as expected with SIR results below the 8 $Log_{10}\Omega s$ pass/ fail criteria, but these vehicles were DI washed with no saponifier. The thesis was to see if the DI could clean the SMT water-soluble flux out from under a low standoff part.
6. The water-soluble flux test on this QFN 48 test vehicle showed 7 $Log_{10}\Omega s$ average, which failed the 8 $Log_{10}\Omega s$ pass / fail criteria but again this was used with no saponifier in the DI water rinse
7. The SIR Test Protocol using a QFN 48 component Test coupon allows one to dial in their material choices for fluxes as well as their manufacturing processes to ensure they have objective evidence that meets Section 8 of the IPC J-STD-001G of how clean or dirty they are underneath their BTC or QFN style components as it relates to surface insulation resistance (SIR).
8. The ability to see and visualize cubic volume of flux residue as it correlates to SIR values is the key to making sure your reflow profile and cleaning process if applicable meets your design expectation for cleanliness underneath your most difficult componets suchs as BTC /LGA's as evidenced by this QFN -48 test coupon.

CONCLUSION

1. The use of a specific component type such as QFN -48 design on a custom SIR test coupon that correlates to actual components on the actual electronic hardware allows the design engineer and process engineer the ability to correlate cleanliness and specifically SIR values underneath the site-specific components to ensure the material choices – SMT paste / touch up fluxes and or selective wave solder fluxes, etc. as well as their corresponding manufacturing processes meet their design and manufacturing SIR/cleanliness objectives.
2. The QFN 48 Test vehicle, as well as its corresponding glass test vehicle, allows the design engineer and manufacturing engineer a unique visual / display of where and how the flux residue pools and fills between ground lug area and its corresponding signal pin area.
3. SIR testing allows one to collect the objective evidence needed to set design rules for different component layouts as well as determine the

influence of reflow temperatures and dwell times needed to achieve optimal outgassing as it correlates to SIR values. This tool allows one to determine the optimal ramp to spike or soak to spike reflow that works best to achieve the best outgassing and highest achievable SIR values.

4. This type of SIR tool also allows one to determine which SMT paste / touch up flux / selective solder flux/wave solder flux, etc. as well as their intermixing (flux residue cocktail) characteristics underneath certain component types. The ability to collect objective evidence and real data to support your material choices and process parameters is key as one move to higher density and smaller pitch component styles and/or BTC style components.
5. The cubic volume of flux increases as the pitch and gap spacing decreases, which correlates into lower SIR values. The ability to measure the SIR value underneath site-specific components is critical in determining acceptable cleanliness levels underneath site-specific difficult style components such as BTC/QFN style components. This corresponding test design layout allows for both the design engineer and process engineer to work together with real SIR data to build their electronic hardware that will meet their end customer cleanliness objectives.
6. One facet of reliability engineering is one's ability to ensure cleanliness underneath your most difficult component types, such as BTC / QFN's. This type of specific component type testing using SIR allows one to gather and record real SIR data underneath these high i/o devices and to dial in your material choice and process parameters to ensure cleanliness and ultimately meet your warranty expectation as it relates to cleanliness underneath your most difficult components.

FOLLOW-ON RESEARCH

The researchers are planning a follow-on study using this board design on a Glass SIR test vehicle. The SIR channels will be sintered with silver. QFN-48 components will be patterned across the four channels. During SIR testing, visual and surface insulation resistance will be captured and reported.

ACKNOWLEDGEMENTS

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REFERENCES

[1]. IPC Joint Industry (2018-September). Standard. *Requirements for Soldered Electrical and Electronic Assemblies.* IPC J-STD-001G Am 1. IPC Bannockburn, IL.

[2]. IP-9202 (2011-October). *Material and Process Characterization/Qualification Test Protocol for Assessing Electrochemical Performance.* IPC Bannockburn, IL.